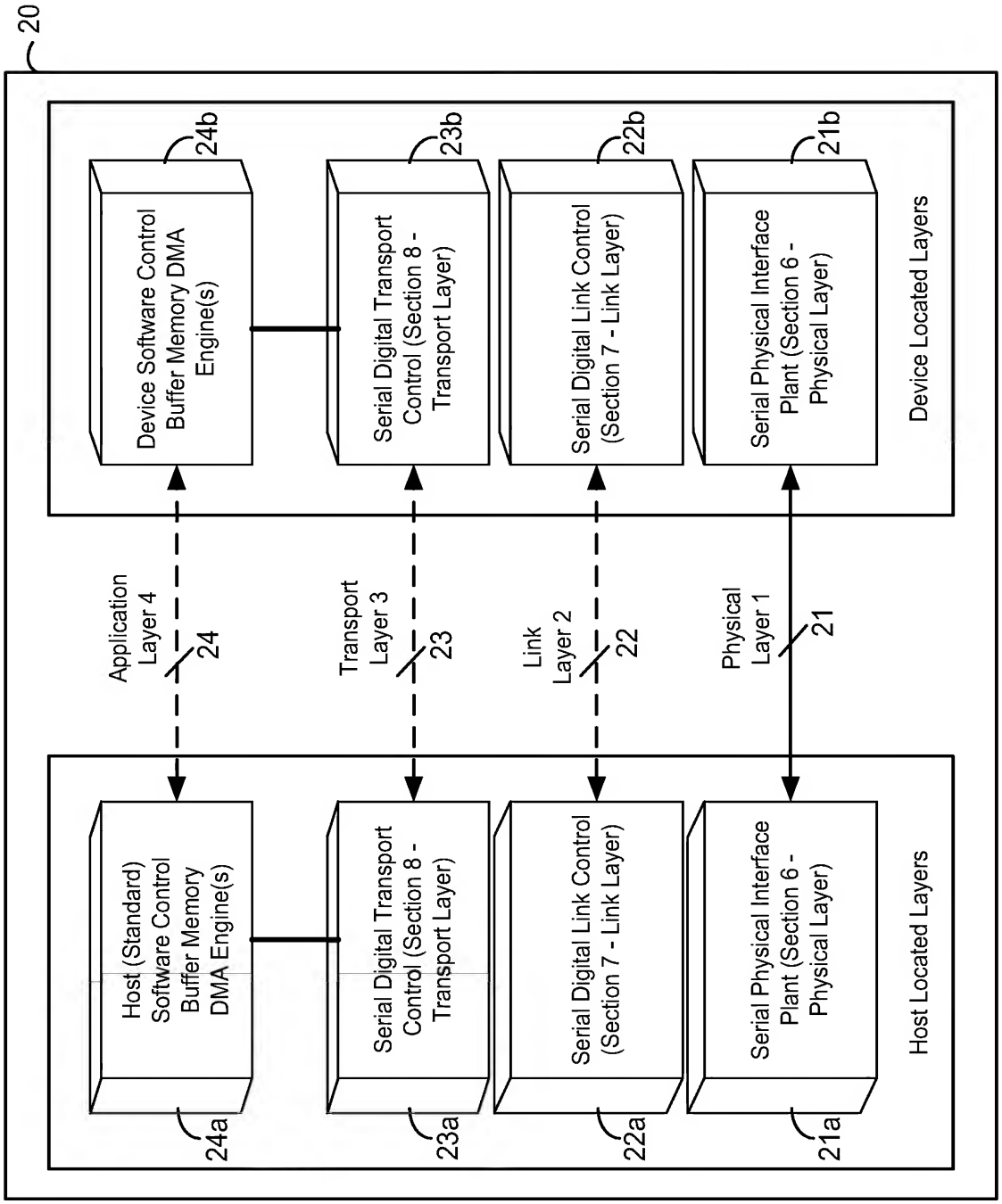


FIG. 1a
(PRIOR ART)

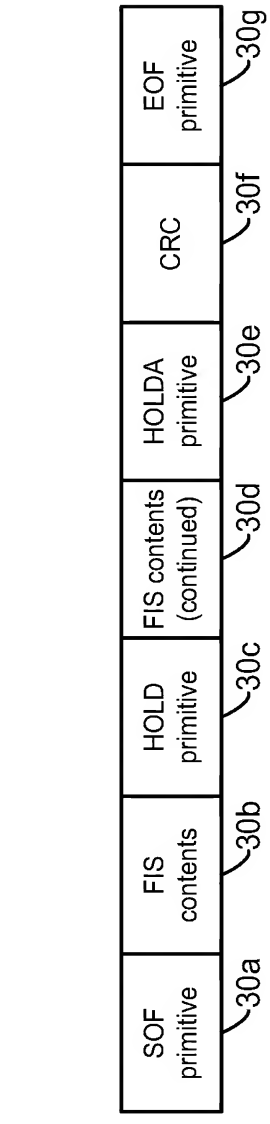


FIG. 1b
(PRIOR ART)

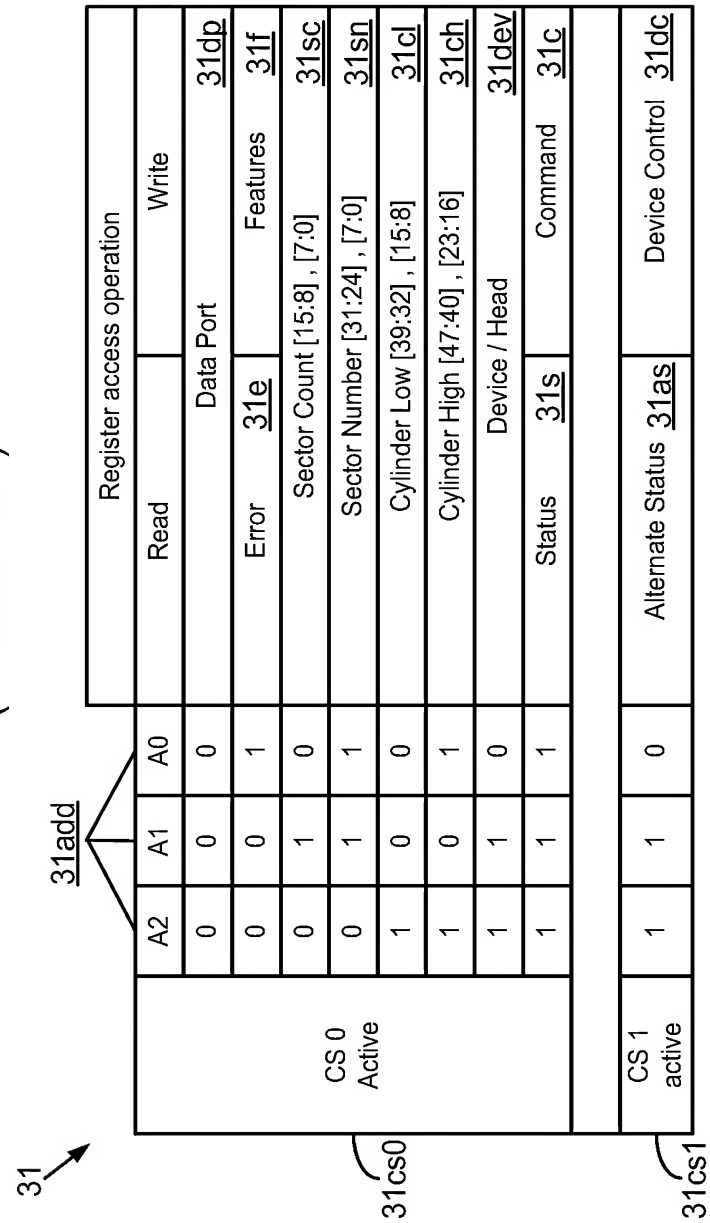


FIG. 1c
(PRIOR ART)

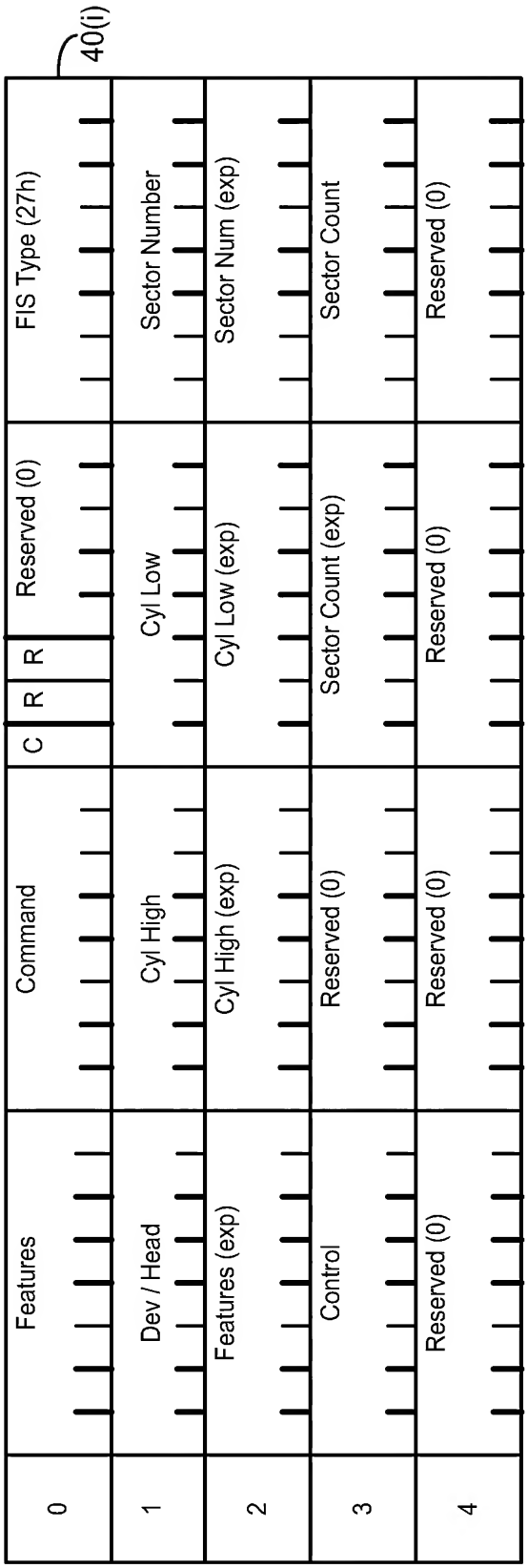


FIG. 1d(i) Register FIS Host to Device

(PRIOR ART)

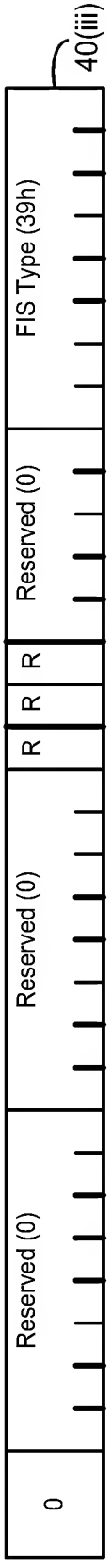


FIG. 1d(iii) DMA Activate FIS, Device to Host

(PRIOR ART)

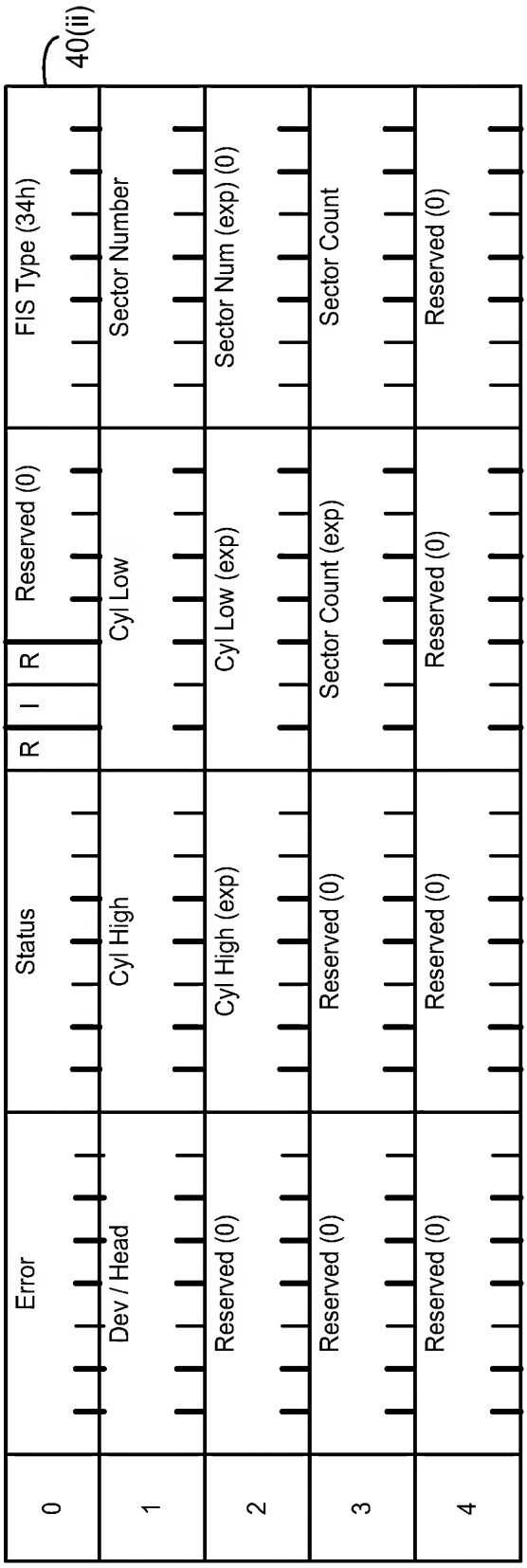


FIG. 1d(ii) Register FIS Device to Host

(PRIOR ART)

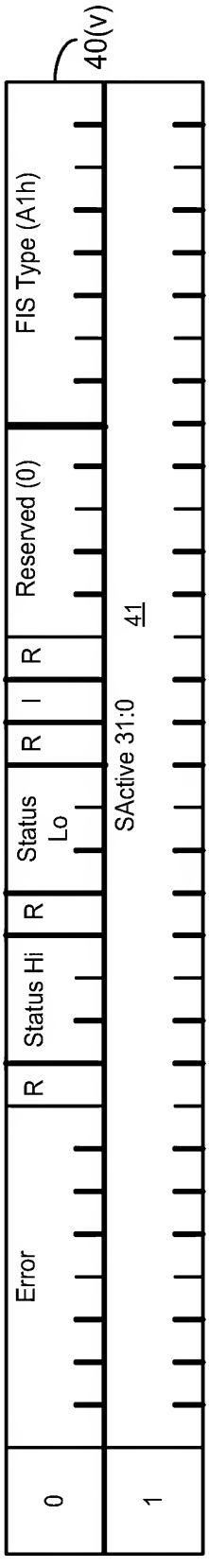


FIG. 1d(v) Set Device Bits FIS

(PRIOR ART)

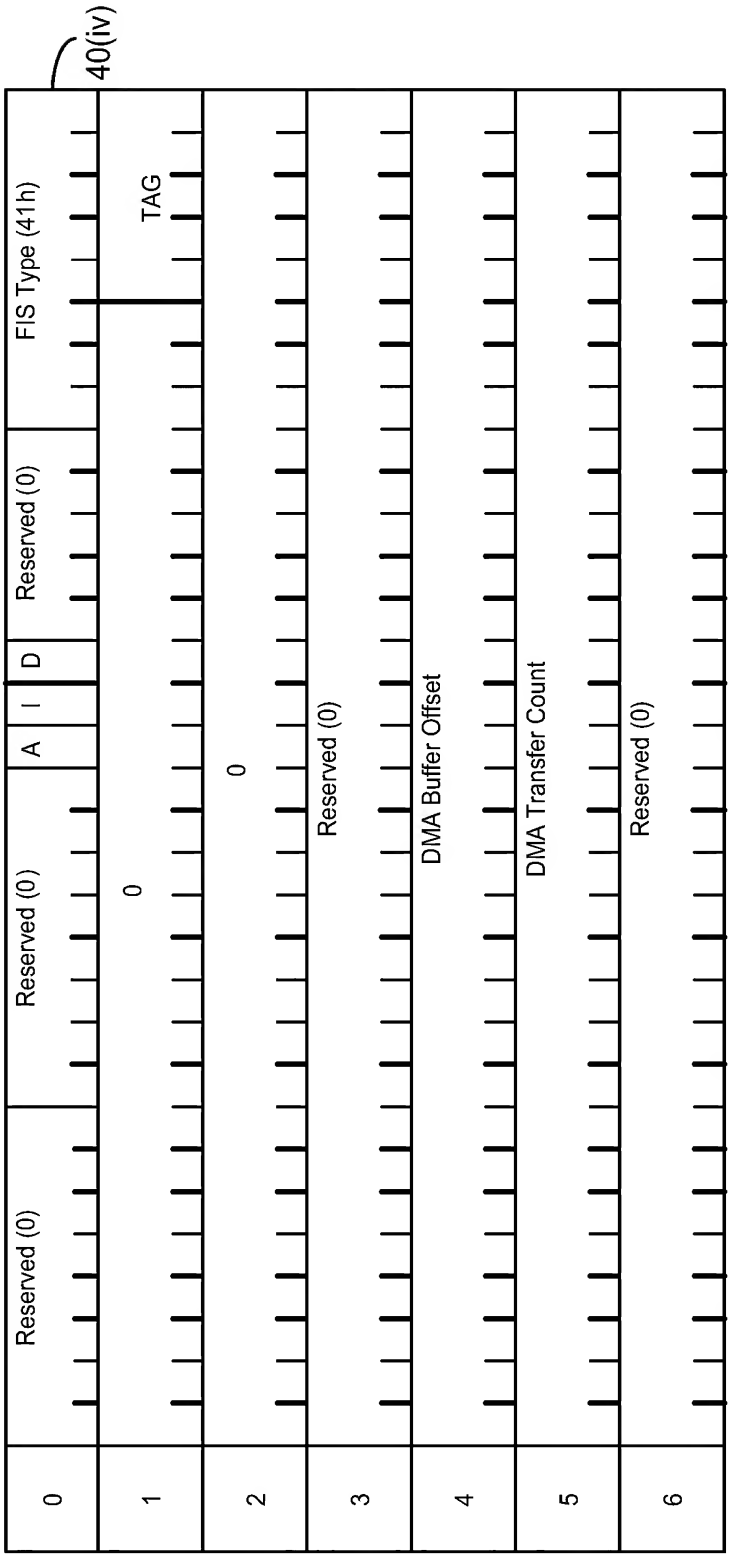


FIG. 1d(iv) DMA Setup FIS

(PRIOR ART)

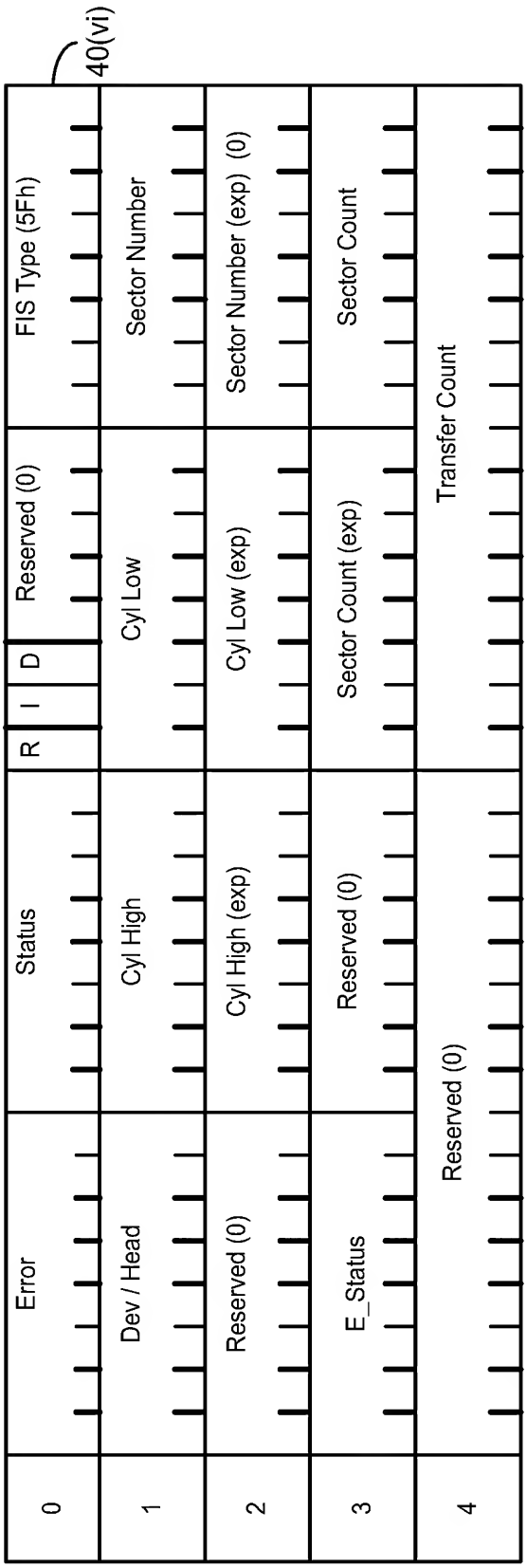


FIG. 1d (vi) PIO Setup FIS
(PRIOR ART)

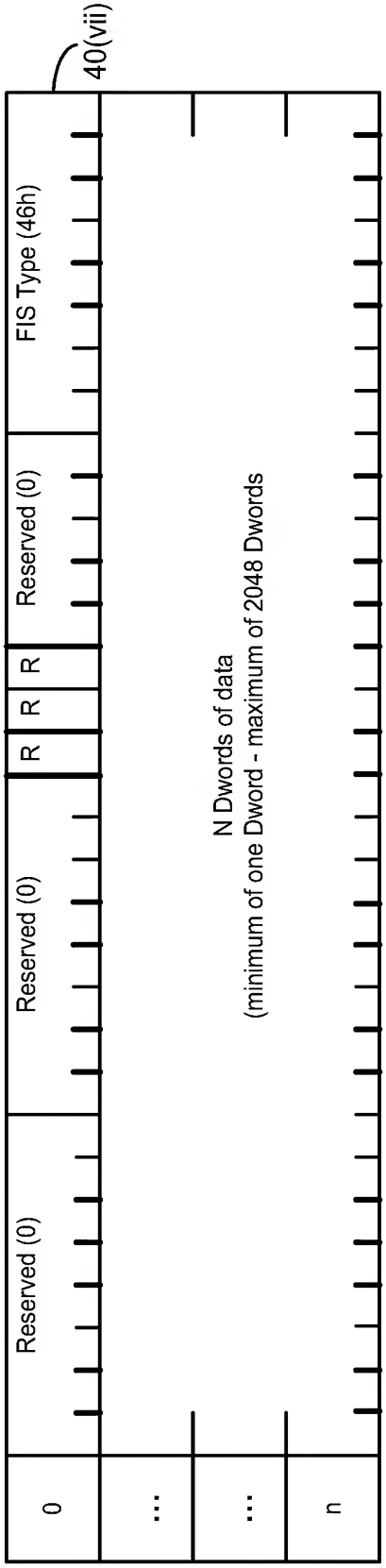


FIG. 1d(vii) Data FIS
(PRIOR ART)

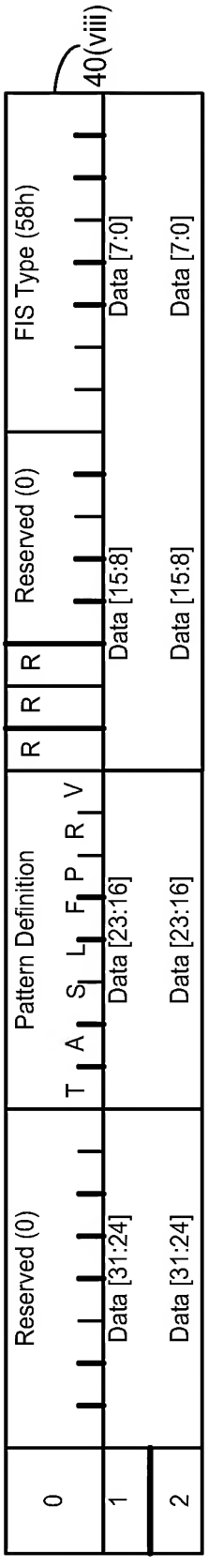


FIG. 1d (viii) BIST Activate FIS

(PRIOR ART)

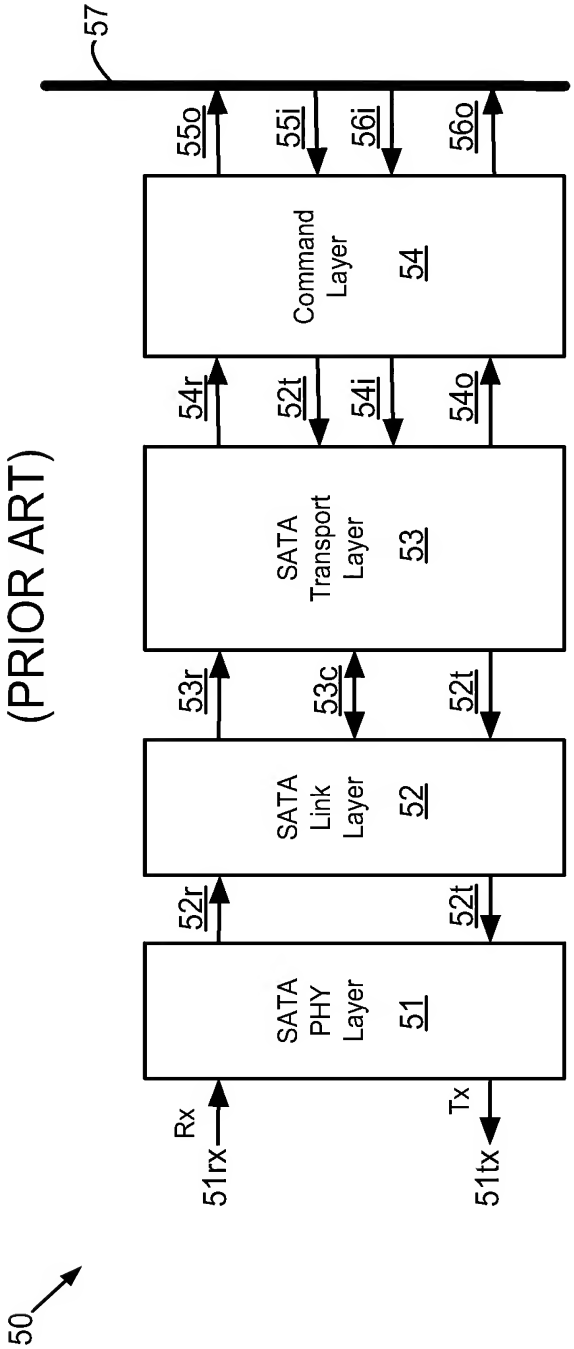


FIG. 2a

(PRIOR ART)

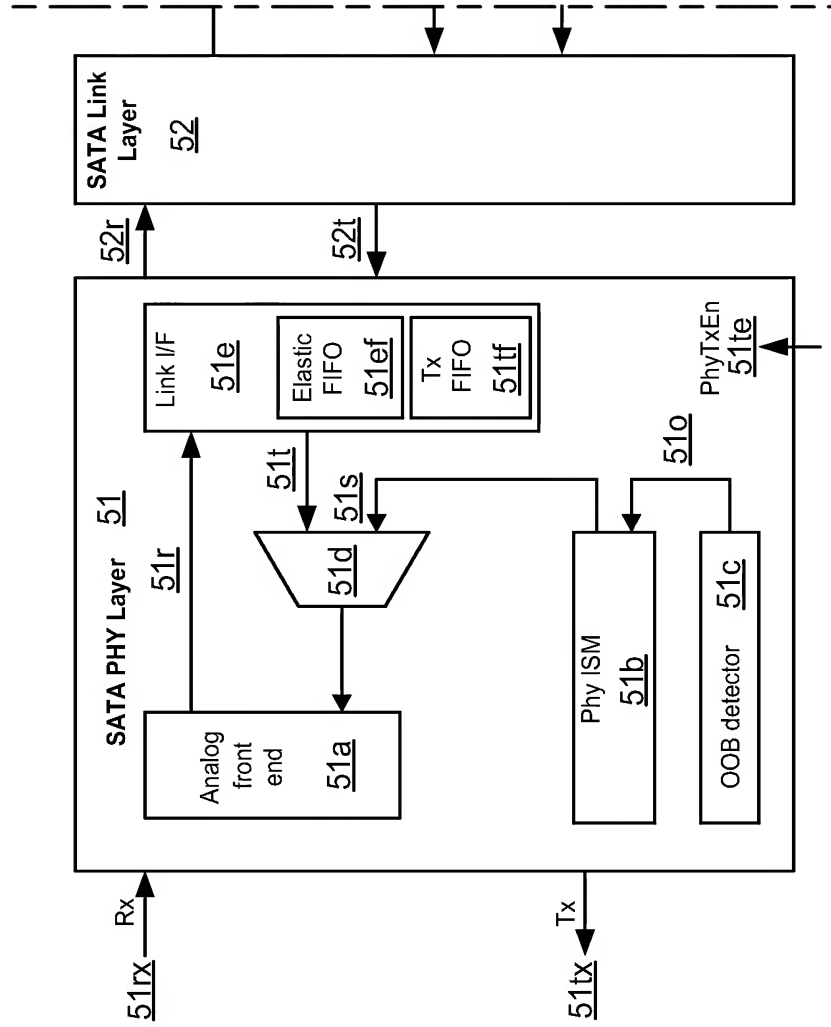
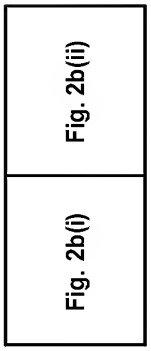


FIG. 2b(i)
(PRIOR ART)



Key To
FIG. 2b

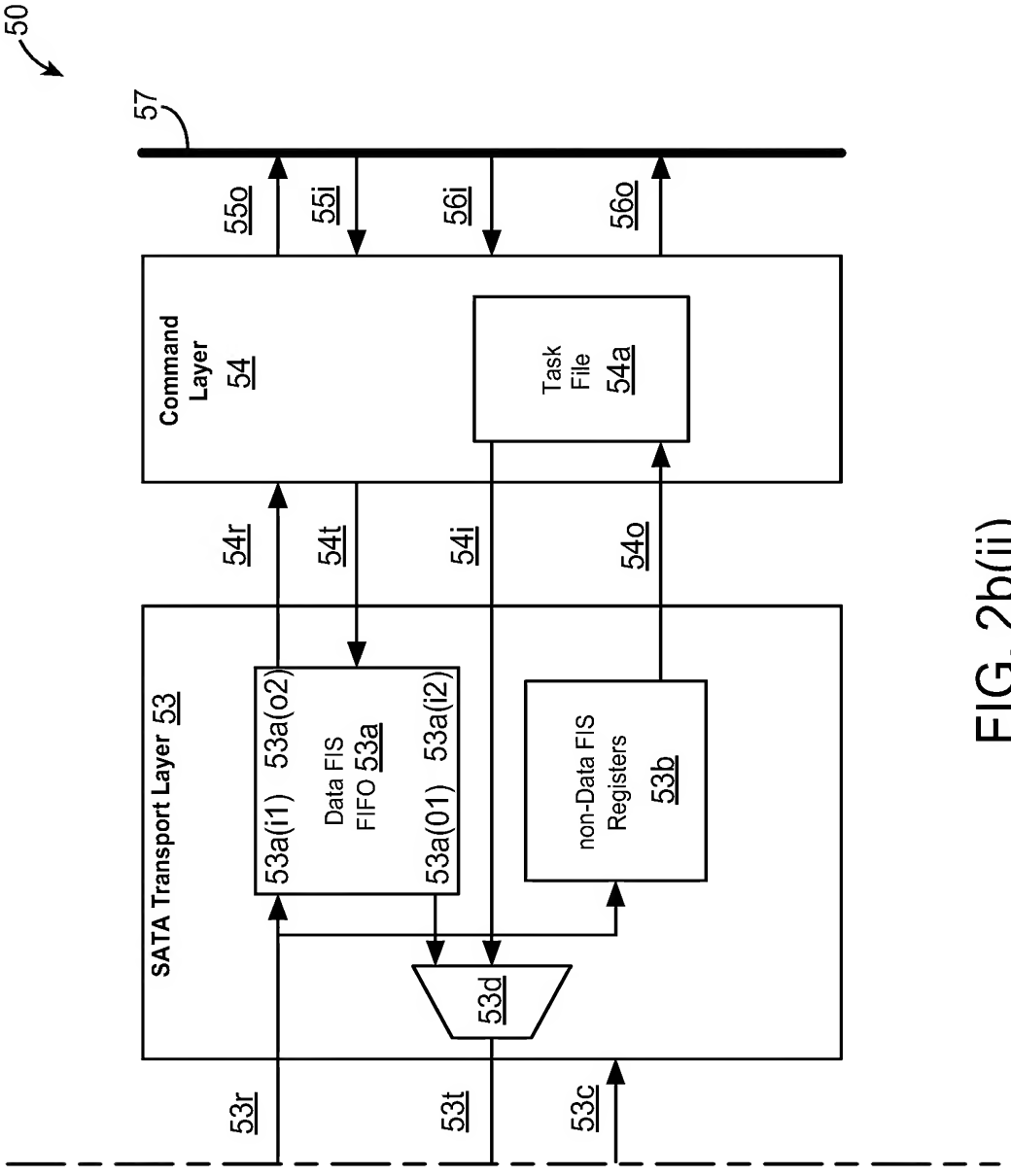


FIG. 2b(ii)
(PRIOR ART)

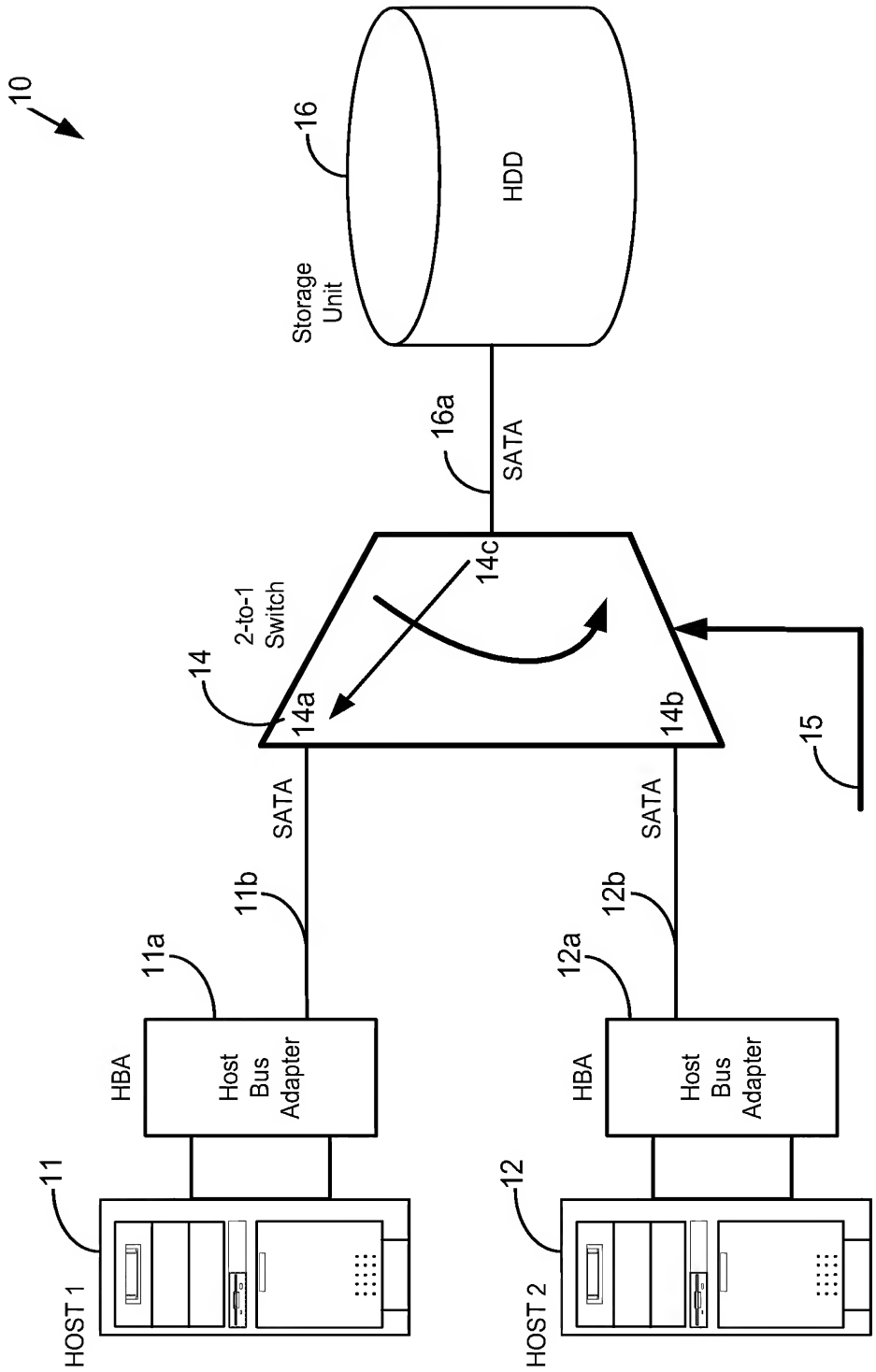


FIG. 3a
(PRIOR ART)

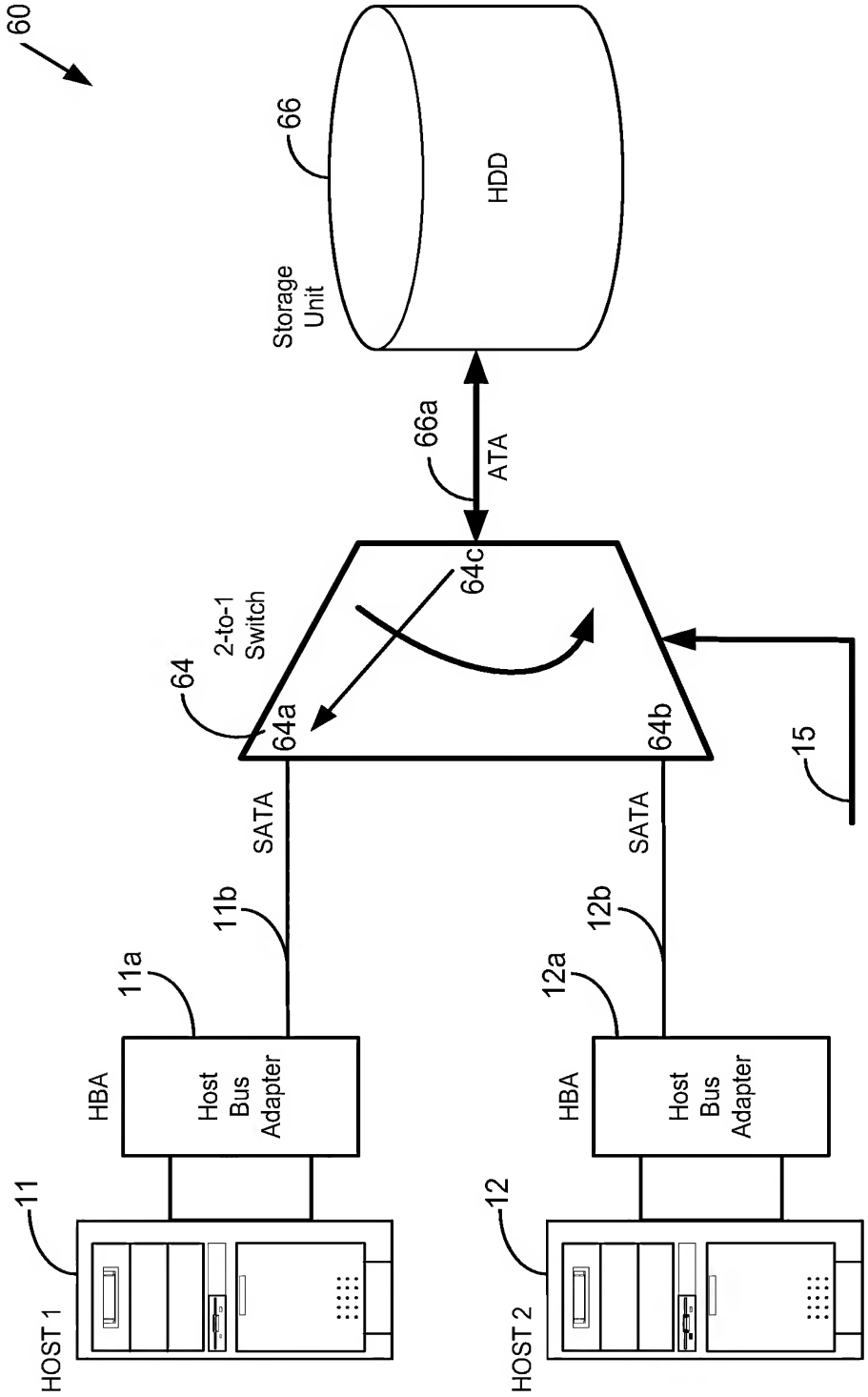


FIG. 3b
(PRIOR ART)

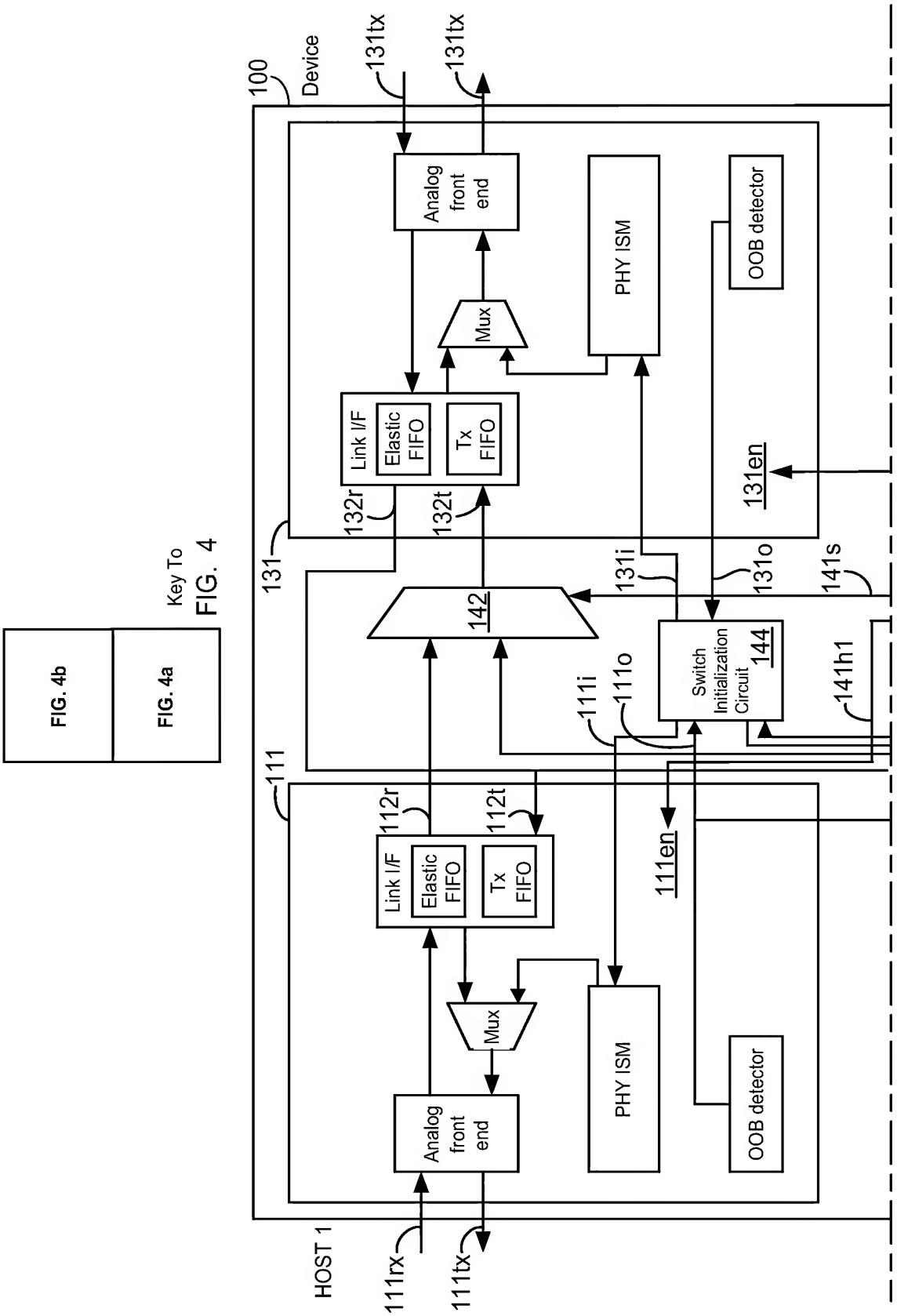

Key To FIG. 4
FIG. 4b
FIG. 4a
100
Device
131tx
131tx
Analog front end
PHY ISM
OOB detector
Mux
Link I/F
Elastic FIFO
Tx FIFO
132r
132t
131en
131
131i
131o
141s
142
Switch Initialization Circuit
144
111i
111o
141h1
111
112r
112t
111en
Mux
PHY ISM
OOB detector
Analog front end
HOST 1
111rx
111tx

FIG. 4a

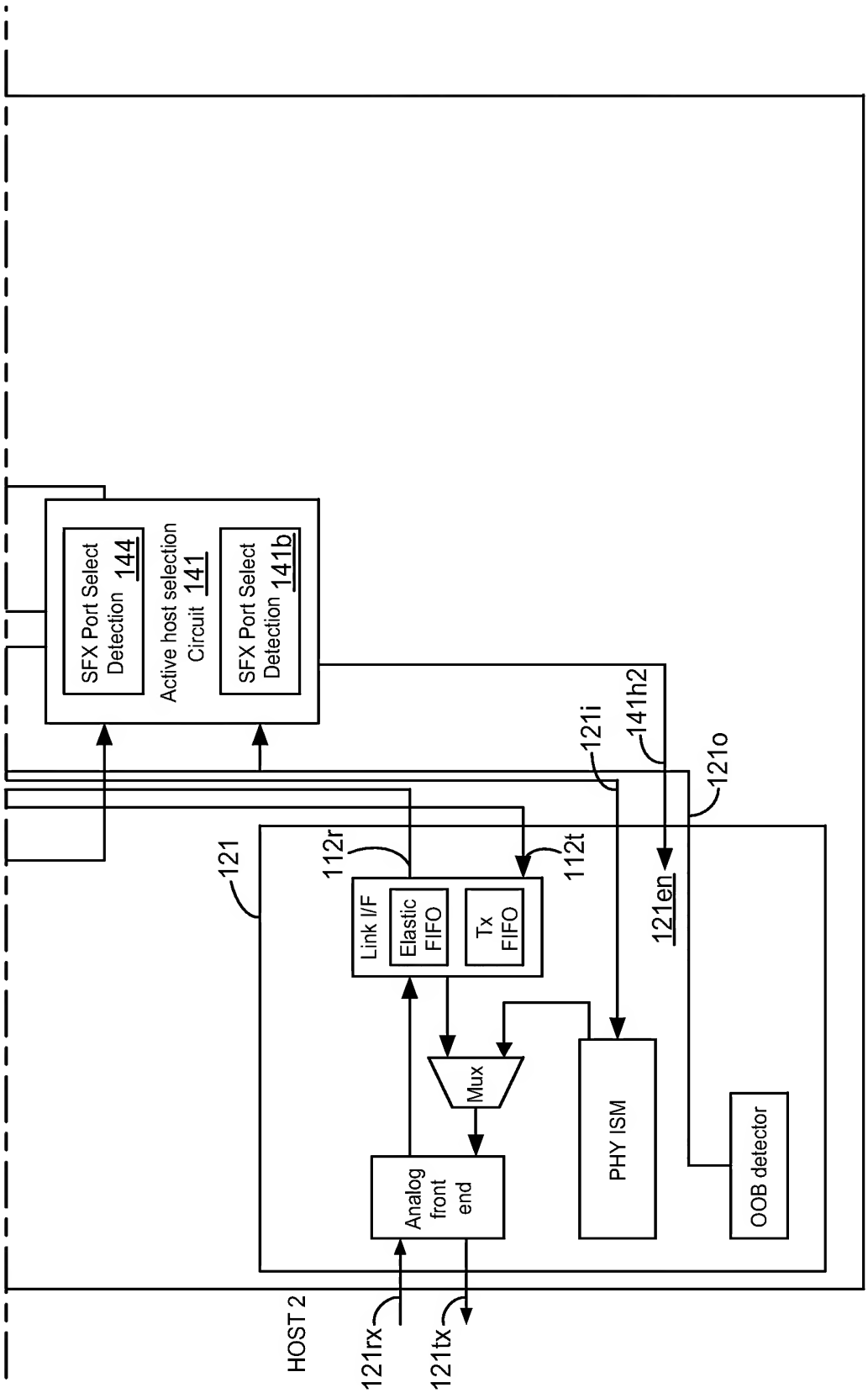

SFX Port Select Detection 144
Active host selection Circuit 141
SFX Port Select Detection 141b
121i
141h2
121o
121
112r
112t
Link I/F
Elastic FIFO
Tx FIFO
121en
Mux
PHY ISM
Analog front end
OOB detector
HOST 2
121rx
121tx

FIG. 4b

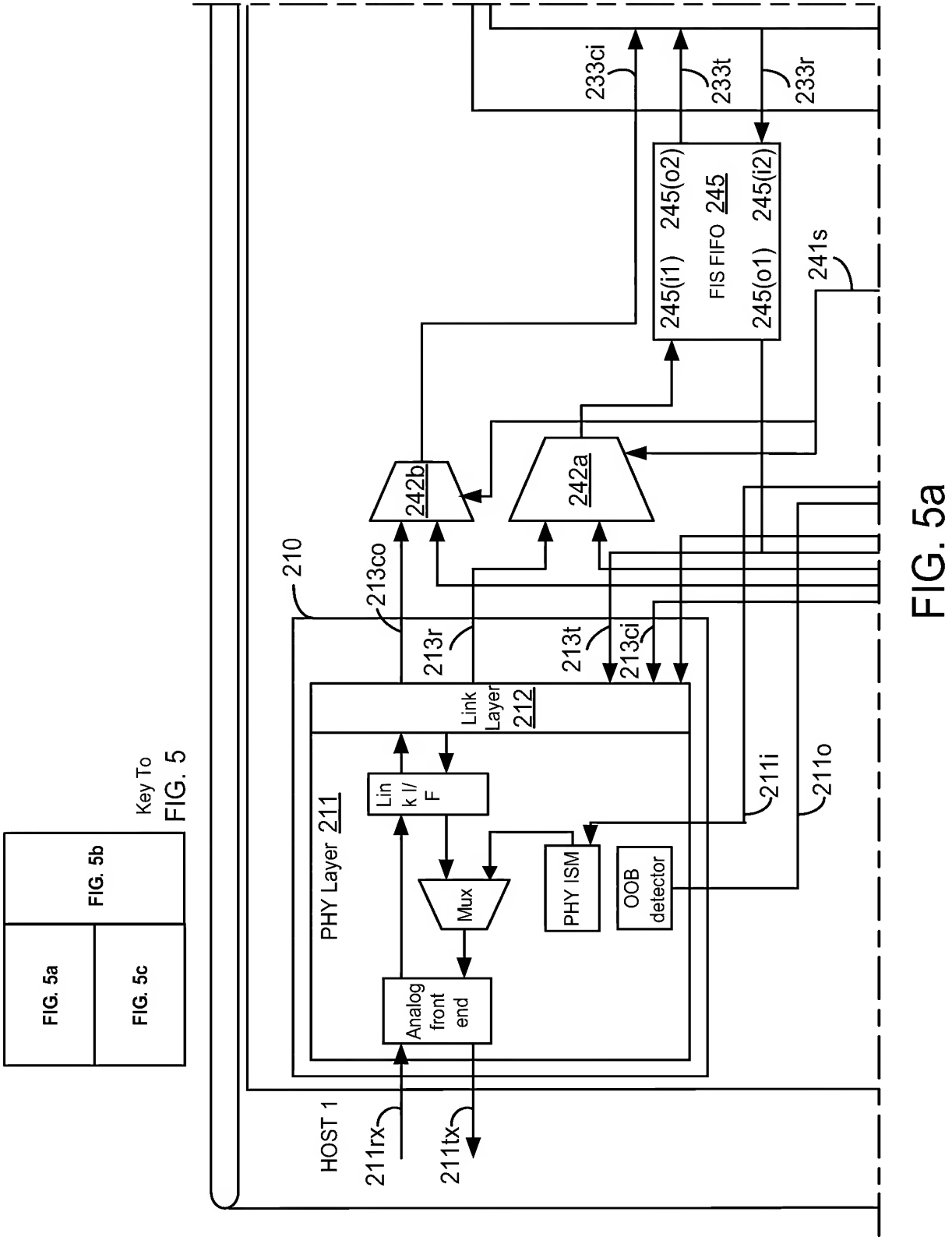


FIG. 5a

Key To FIG. 5

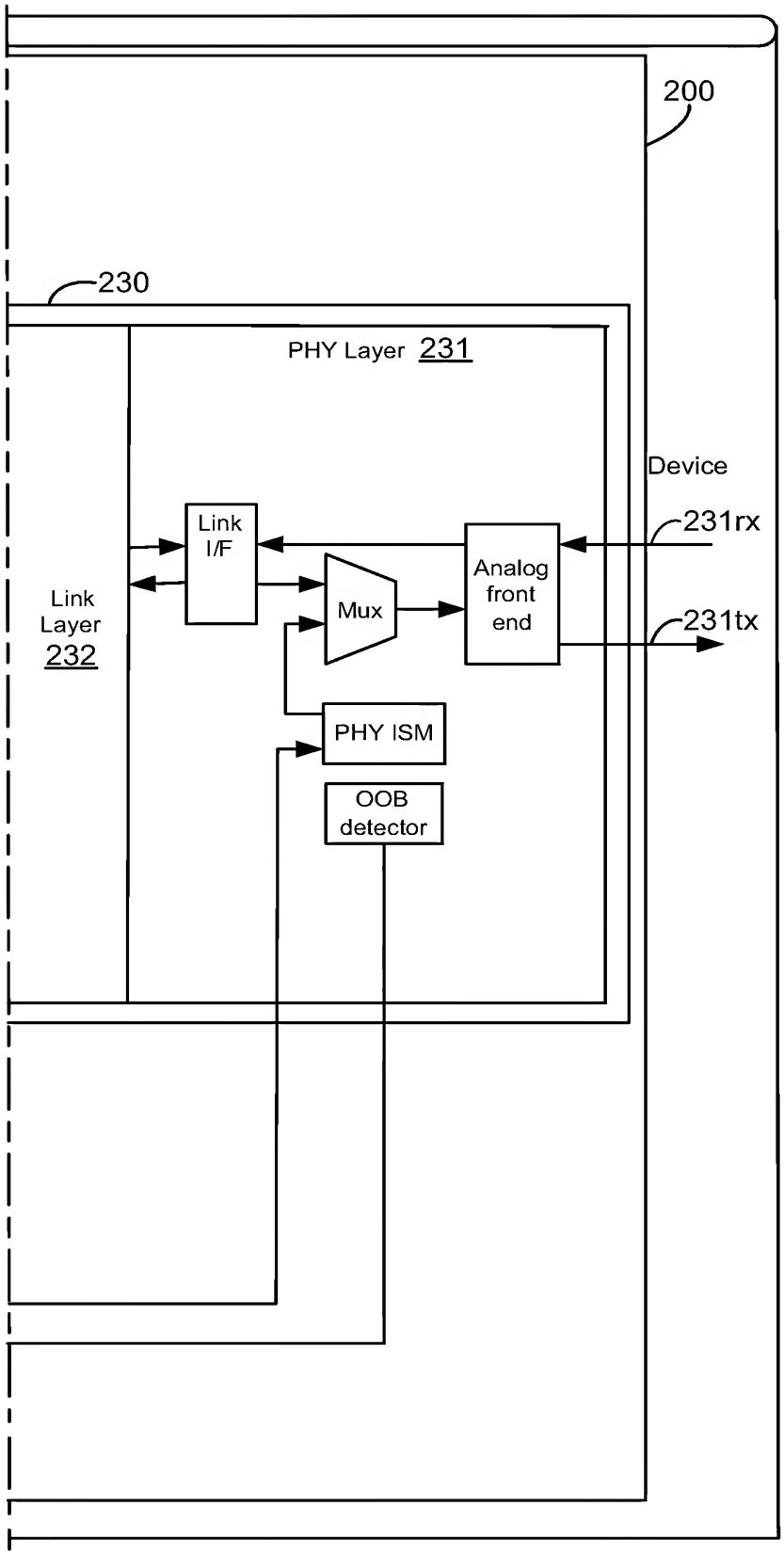

200
230
PHY Layer 231
Device
Link I/F
231rx
Analog front end
Mux
231tx
Link Layer 232
PHY ISM
OOB detector

FIG. 5b

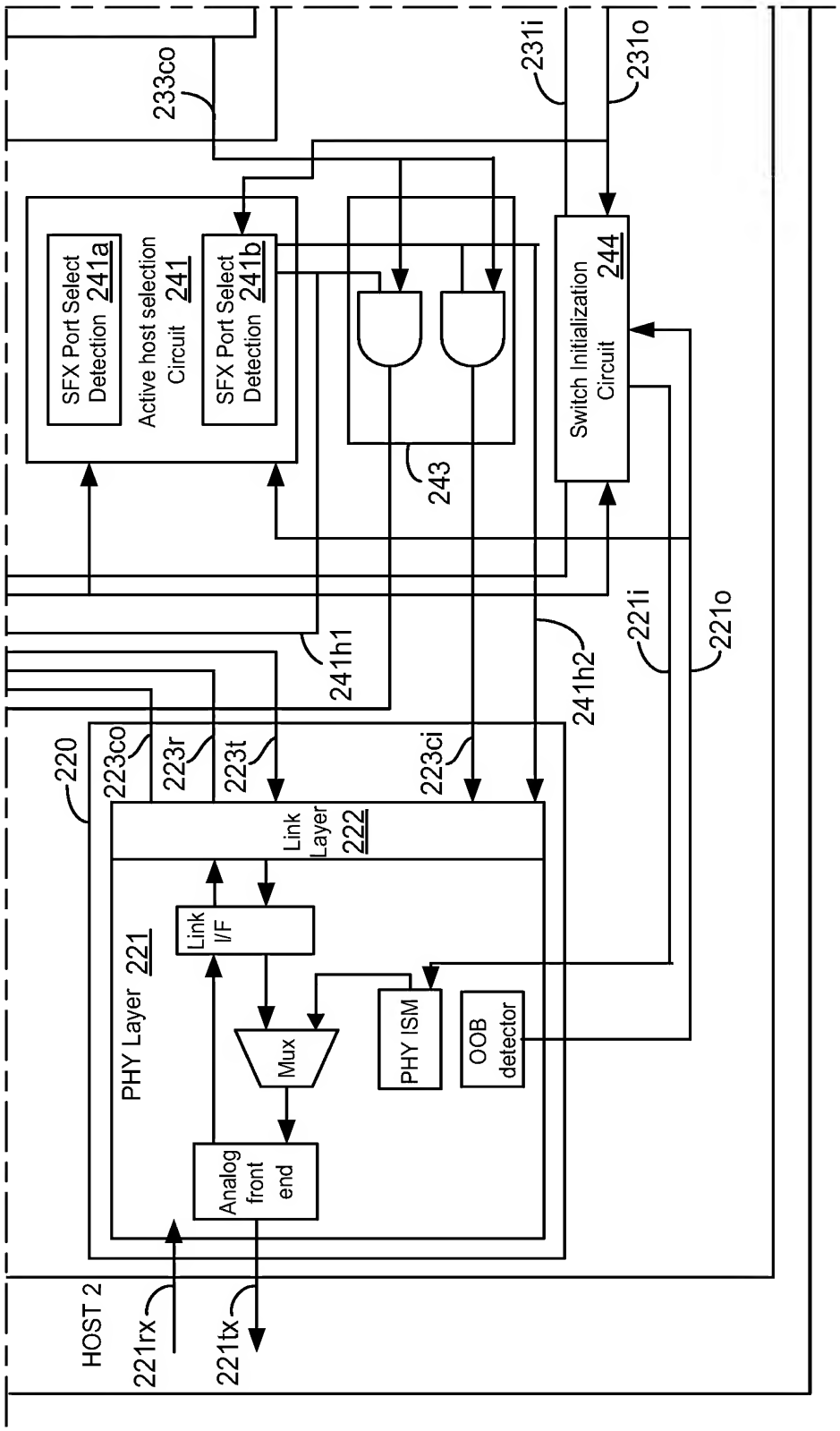

233co
231i
231o
SFX Port Select Detection 241a
Active host selection Circuit 241
SFX Port Select Detection 241b
243
Switch Initialization Circuit 244
241h1
241h2
221i
221o
220
223co
223r
223t
223ci
Link Layer 222
PHY Layer 221
Link I/F
Mux
PHY ISM
OOB detector
Analog front end
HOST 2
221rx
221tx

FIG. 5c

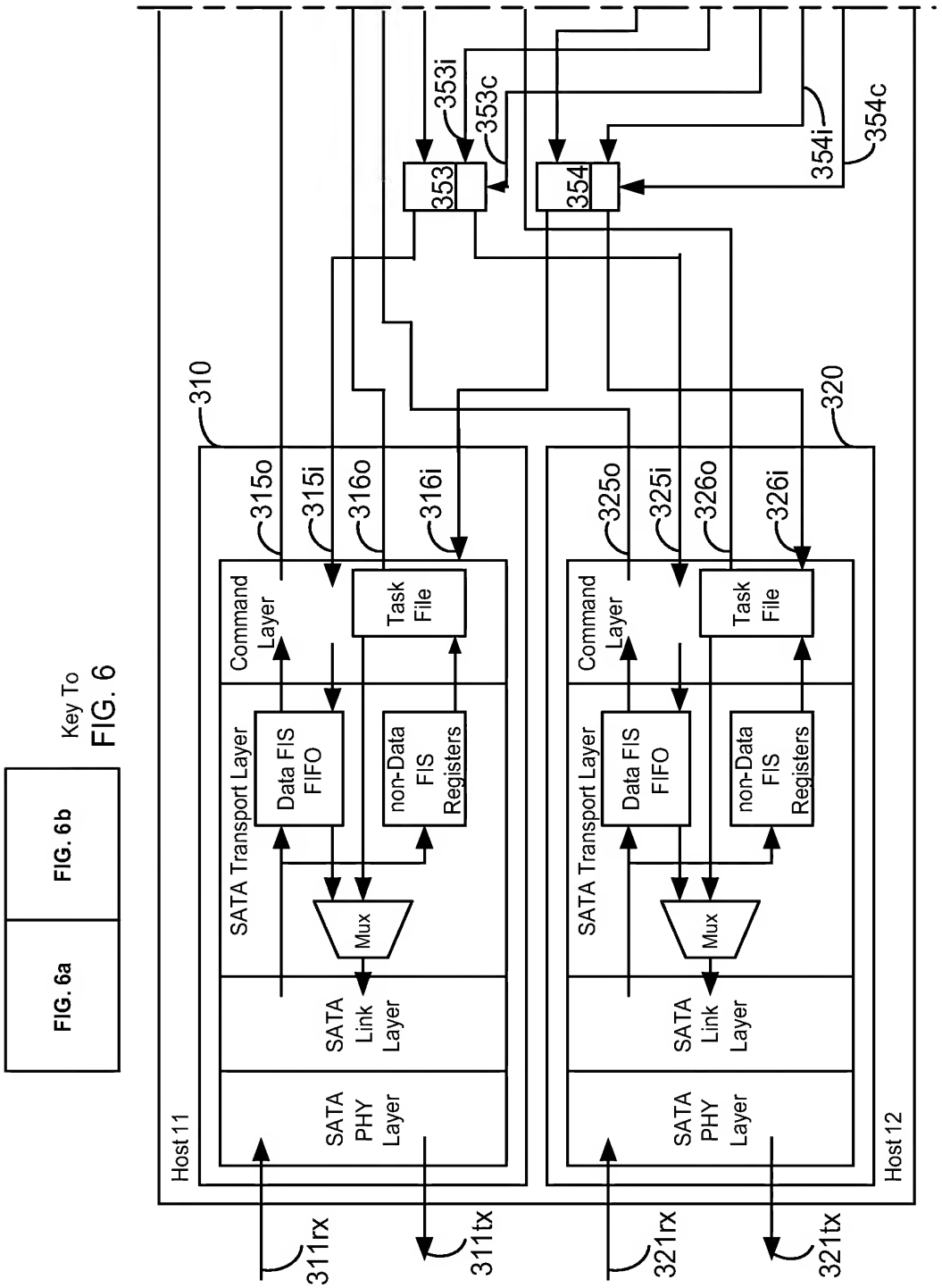


FIG. 6a

Key To FIG. 6

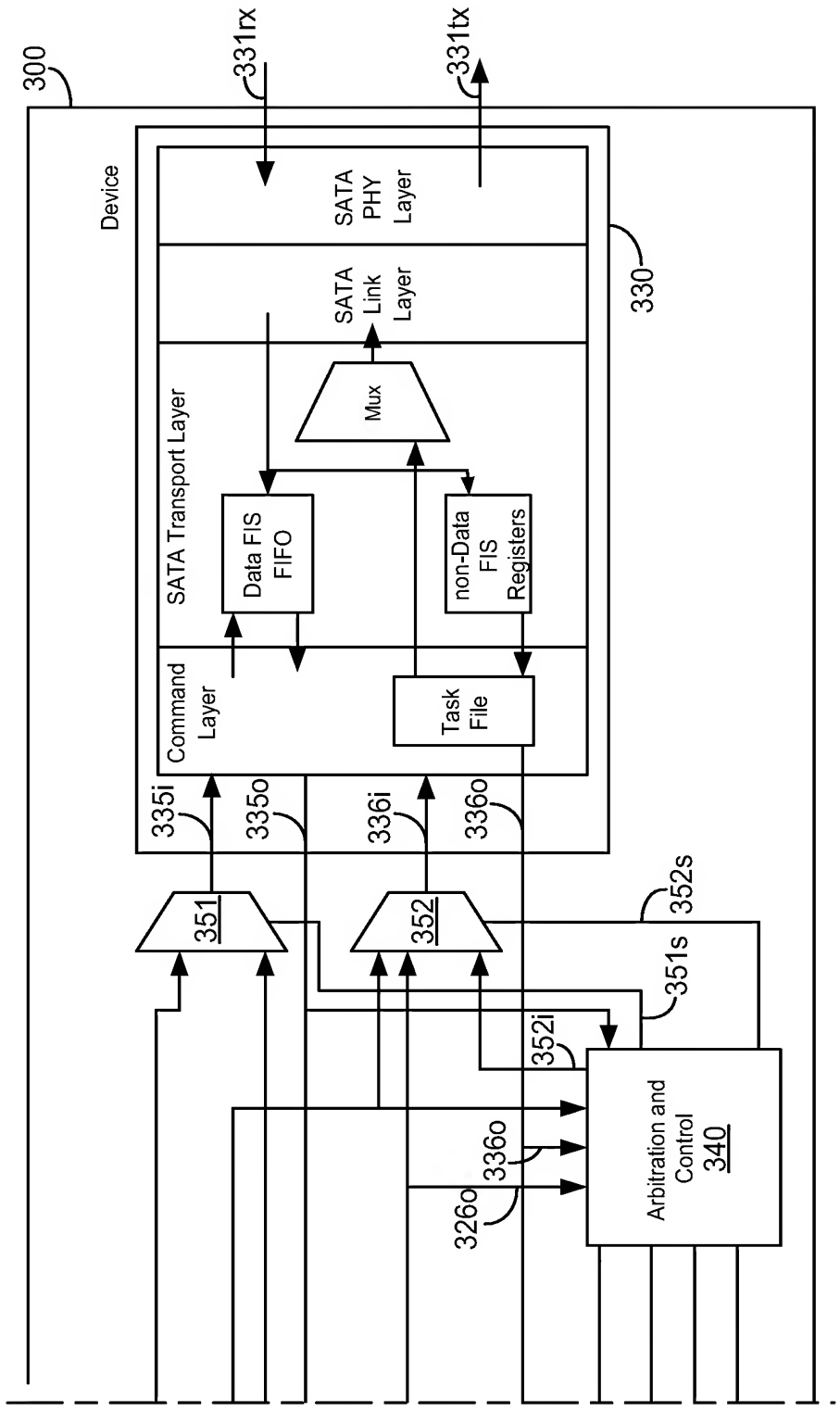

300
331rx
331tx
Device
SATA PHY Layer
SATA Link Layer
330
SATA Transport Layer
Mux
Data FIS FIFO
non-Data FIS Registers
Command Layer
Task File
335i
335o
336i
336o
351
352
352s
351s
352i
Arbitration and Control
340
336o
326o

FIG. 6b

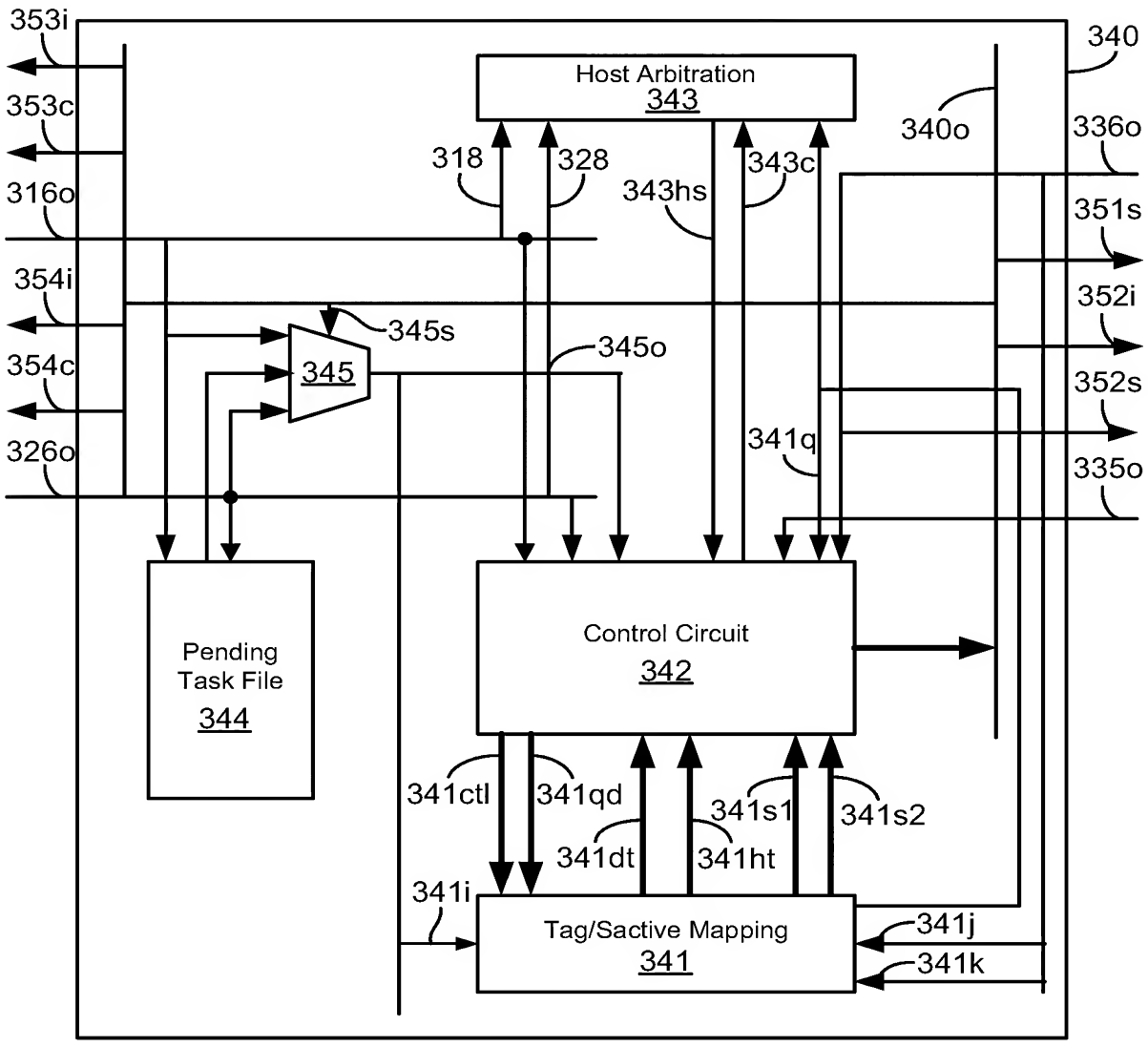

353i
353c
316o
354i
354c
326o
340
340o
336o
351s
352i
352s
335o
341q
318
328
343hs
343c
345s
345o
345
Host Arbitration
343
Pending
Task File
344
Control Circuit
342
341ctl
341qd
341dt
341ht
341s1
341s2
341i
Tag/Sactive Mapping
341
341j
341k

FIG. 7a

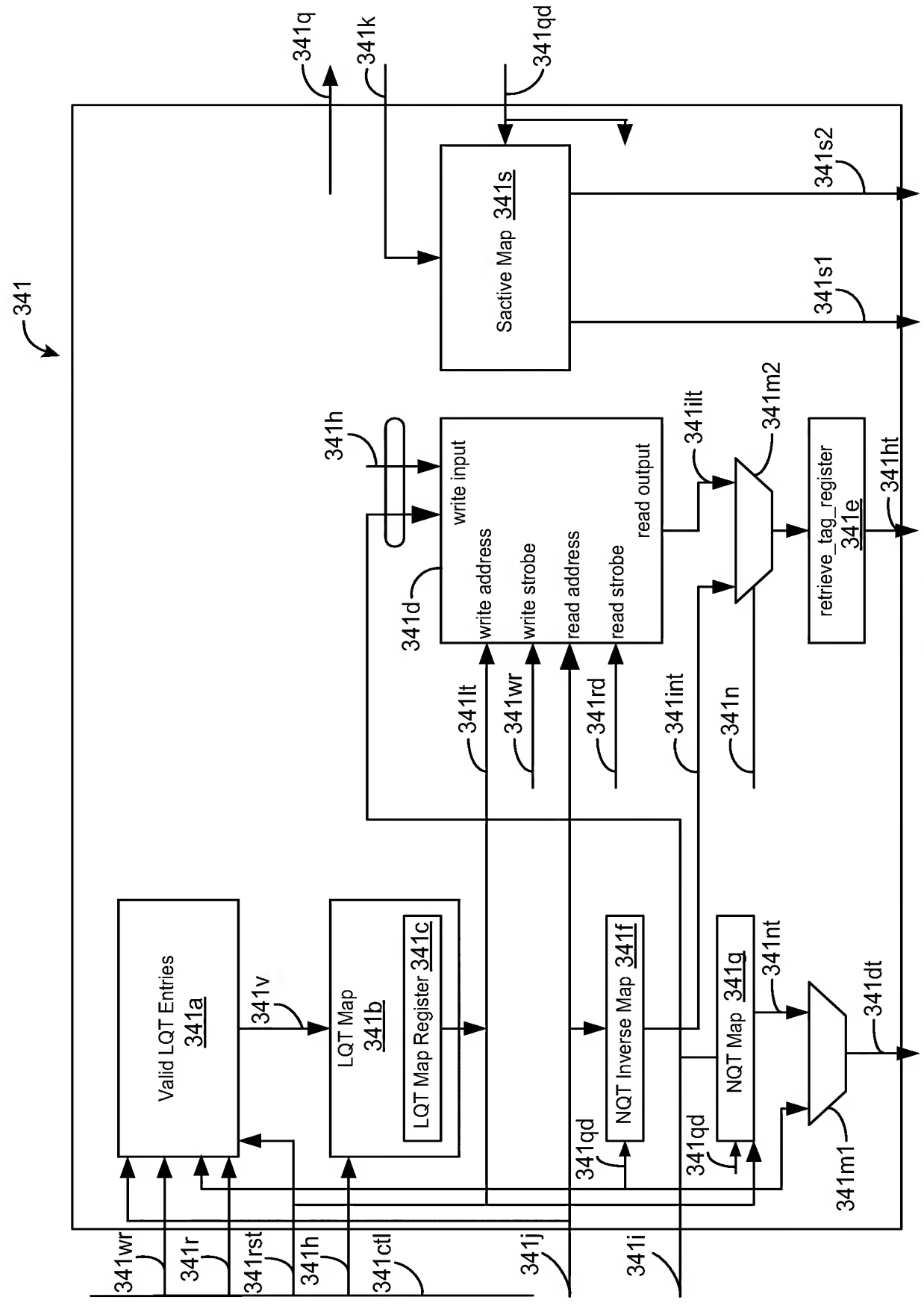

341
341q
341k
341qd
Sactive Map 341s
341s2
341s1
341h
write input
write address
write strobe
read address
read strobe
read output
341d
341ilt
341m2
retrieve_tag_register 341e
341ht
341lt
341wr
341rd
341int
341n
Valid LQT Entries 341a
341v
LQT Map 341b
LQT Map Register 341c
NQT Inverse Map 341f
NQT Map 341g
341nt
341dt
341m1
341qd
341qd
341wr
341r
341rst
341h
341ctl
341j
341i

FIG. 7b

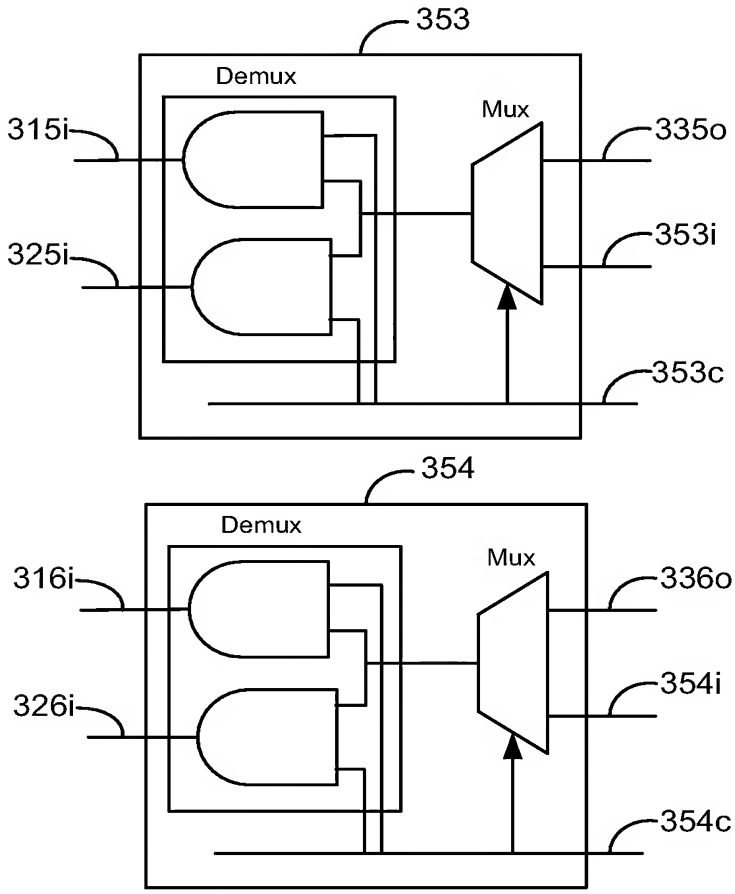

353
Demux
Mux
315i
325i
335o
353i
353c
354
Demux
Mux
316i
326i
336o
354i
354c

FIG. 7c

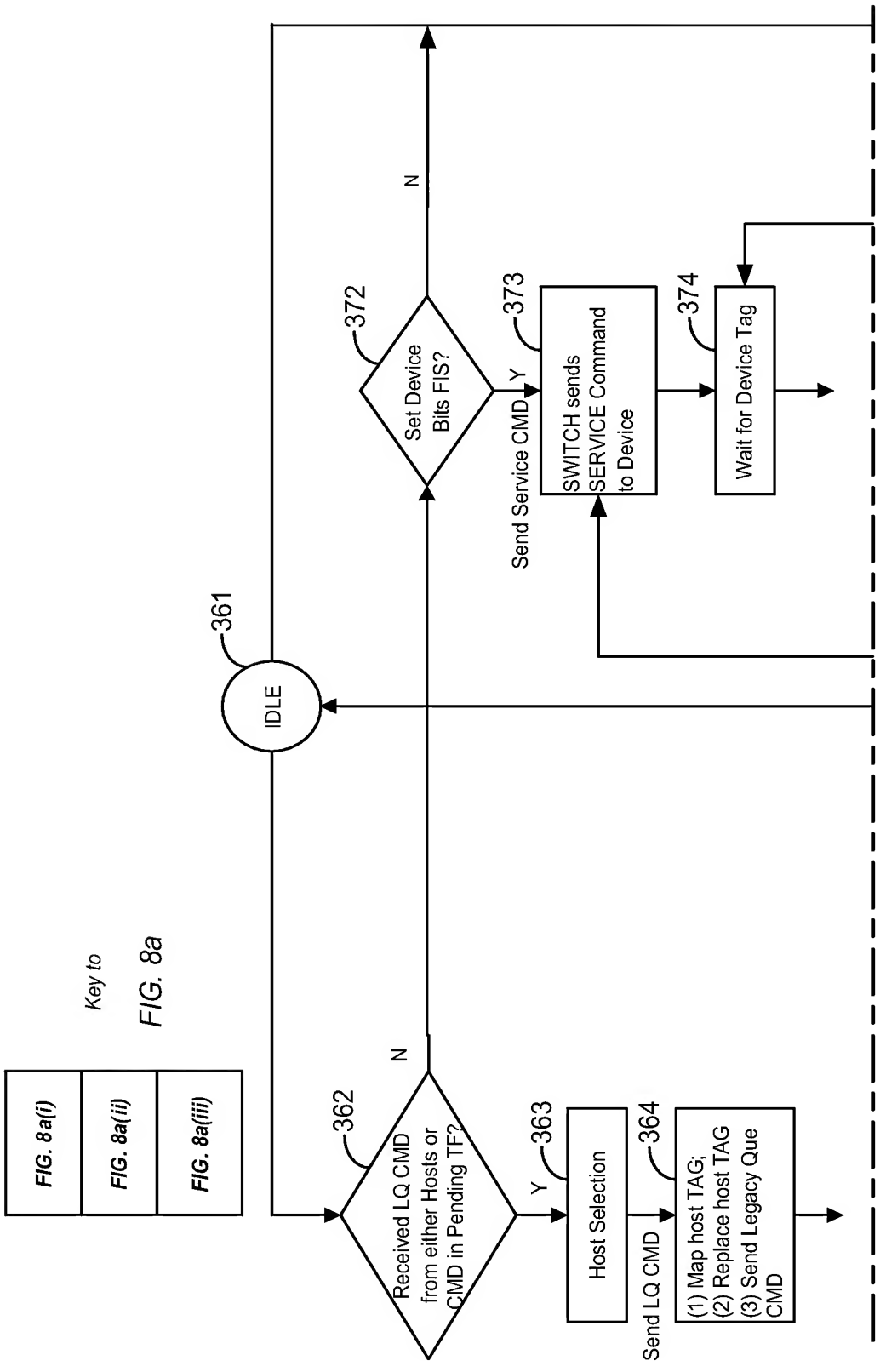


FIG. 8a(i)
FIG. 8a(ii)
FIG. 8a(iii)
Key to
FIG. 8a
361
IDLE
362
Received LQ CMD from either Hosts or CMD in Pending TF?
N
Y
363
Host Selection
364
Send LQ CMD
(1) Map host TAG;
(2) Replace host TAG
(3) Send Legacy Que CMD
372
Set Device Bits FIS?
N
Y
373
Send Service CMD
SWITCH sends SERVICE Command to Device
374
Wait for Device Tag

FIG. 8a(i)

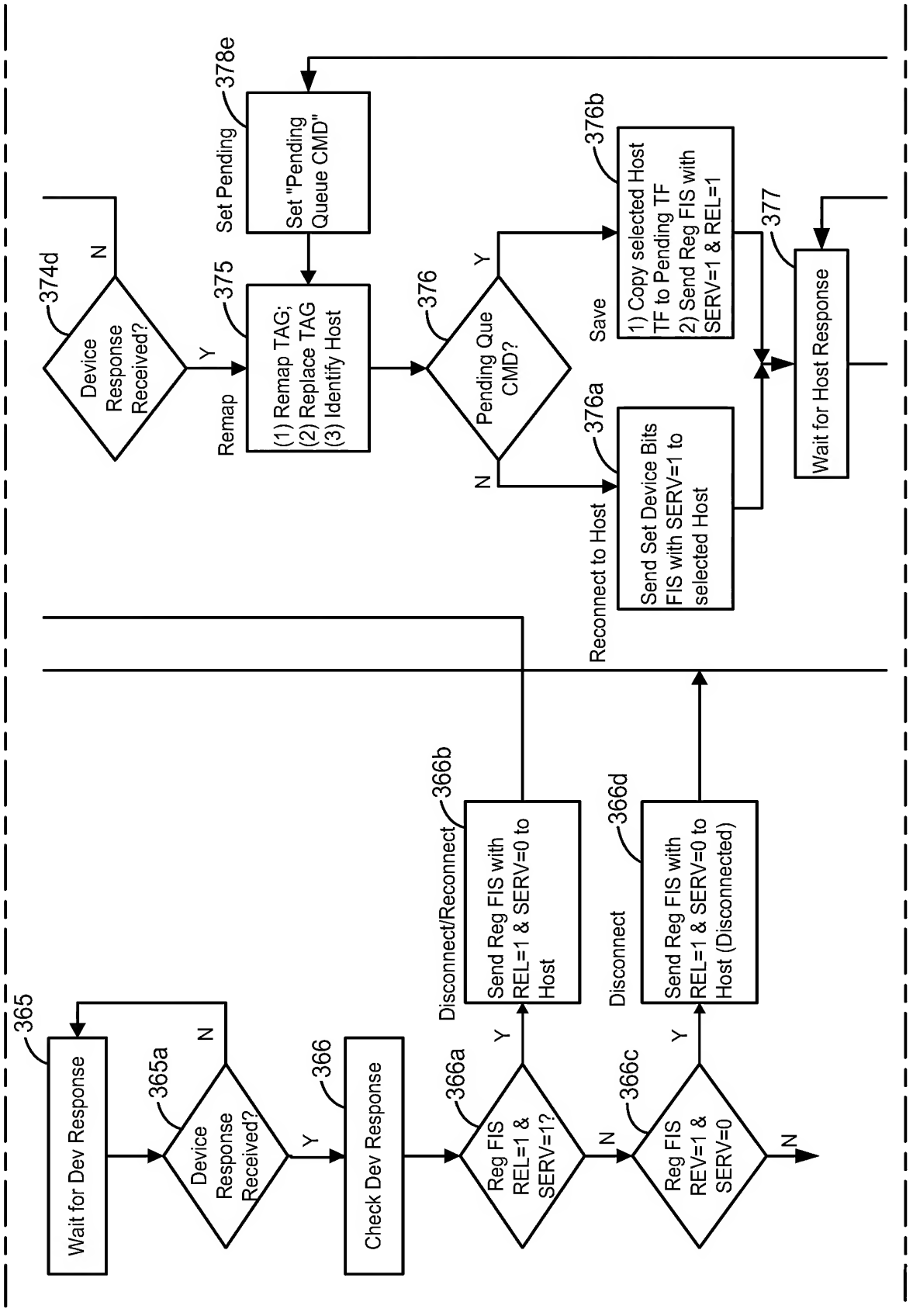

365
Wait for Dev Response
365a
Device Response Received?
N
Y
366
Check Dev Response
366a
Reg FIS REL=1 & SERV=1?
Y
366b
Disconnect/Reconnect
Send Reg FIS with REL=1 & SERV=0 to Host
N
366c
Reg FIS REV=1 & SERV=0
Y
366d
Disconnect
Send Reg FIS with REL=1 & SERV=0 to Host (Disconnected)
N
374d
Device Response Received?
N
Y
375
Remap
(1) Remap TAG;
(2) Replace TAG
(3) Identify Host
376
Pending Que CMD?
Y
N
376a
Reconnect to Host
Send Set Device Bits FIS with SERV=1 to selected Host
376b
Save
1) Copy selected Host TF to Pending TF
2) Send Reg FIS with SERV=1 & REL=1
377
Wait for Host Response
378e
Set Pending
Set "Pending Queue CMD"

FIG. 8a(ii)

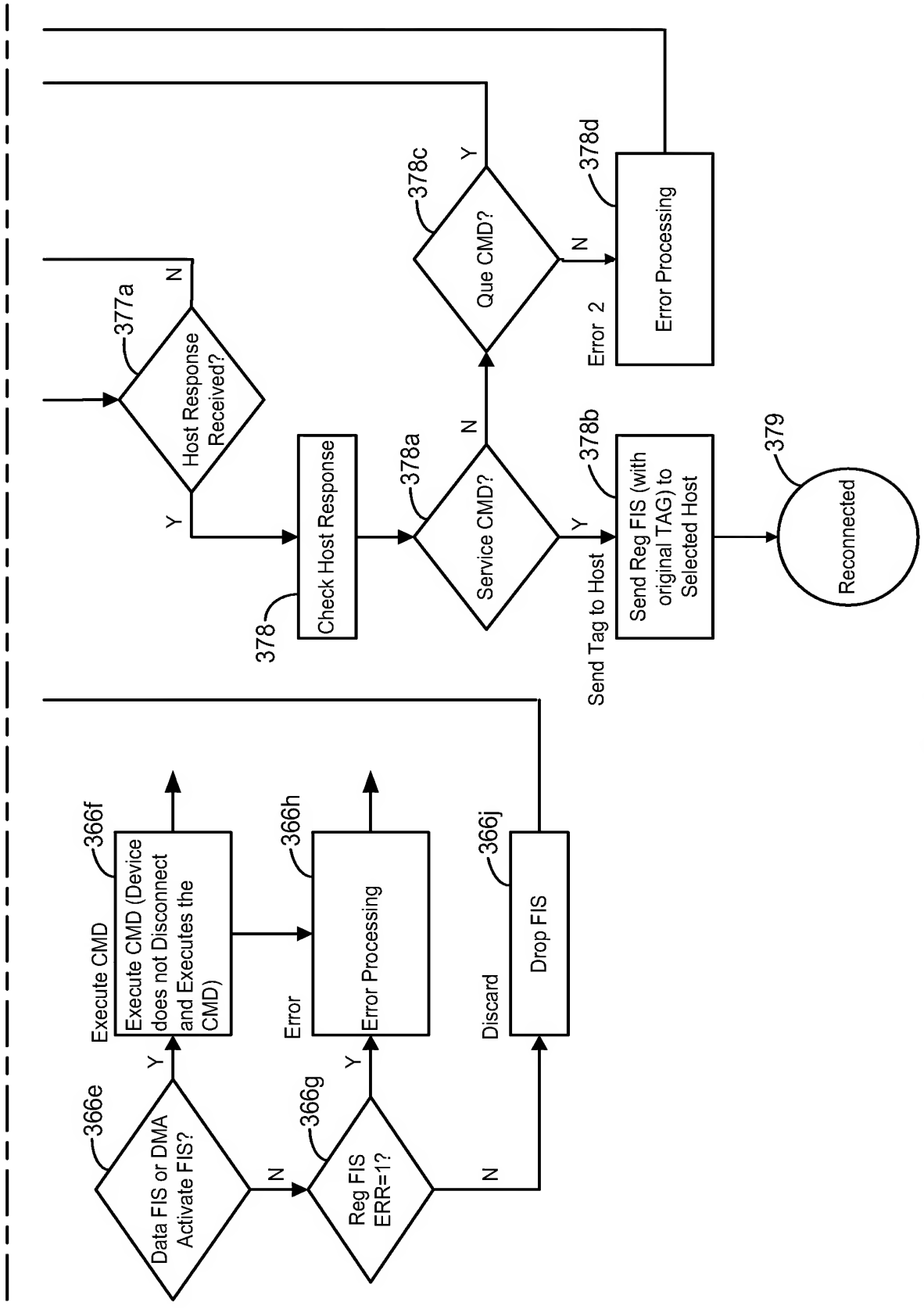

Data FIS or DMA Activate FIS?
366e
Y
N
Execute CMD
Execute CMD (Device does not Disconnect and Executes the CMD)
366f
Reg FIS ERR=1?
366g
Y
N
Error
Error Processing
366h
Discard
Drop FIS
366j
Host Response Received?
377a
N
Y
Check Host Response
378
Service CMD?
378a
N
Y
Send Tag to Host
Send Reg FIS (with original TAG) to Selected Host
378b
Reconnected
379
Que CMD?
378c
Y
N
Error 2
Error Processing
378d

FIG. 8a(iii)

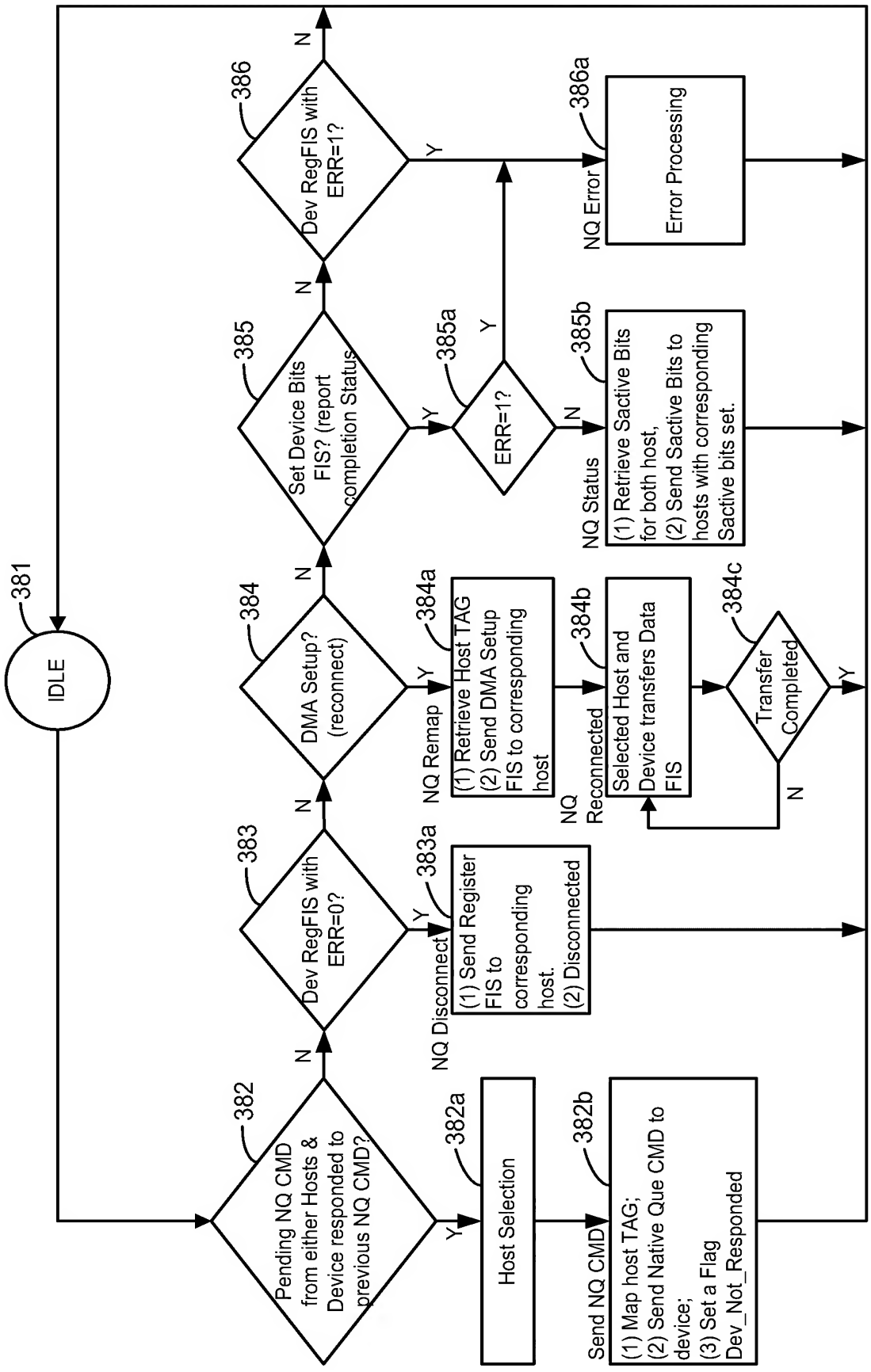

381
IDLE
382
Pending NQ CMD from either Hosts & Device responded to previous NQ CMD?
382a
Host Selection
382b
Send NQ CMD
(1) Map host TAG;
(2) Send Native Que CMD to device;
(3) Set a Flag Dev_Not_Responded
383
Dev RegFIS with ERR=0?
383a
NQ Disconnect
(1) Send Register FIS to corresponding host.
(2) Disconnected
384
DMA Setup? (reconnect)
384a
NQ Remap
(1) Retrieve Host TAG
(2) Send DMA Setup FIS to corresponding host
384b
NQ Reconnected
Selected Host and Device transfers Data FIS
384c
Transfer Completed
385
Set Device Bits FIS? (report completion Status
385a
ERR=1?
385b
NQ Status
(1) Retrieve Sactive Bits for both host,
(2) Send Sactive Bits to hosts with corresponding Sactive bits set.
386
Dev RegFIS with ERR=1?
386a
NQ Error
Error Processing
Y
N

FIG. 8b

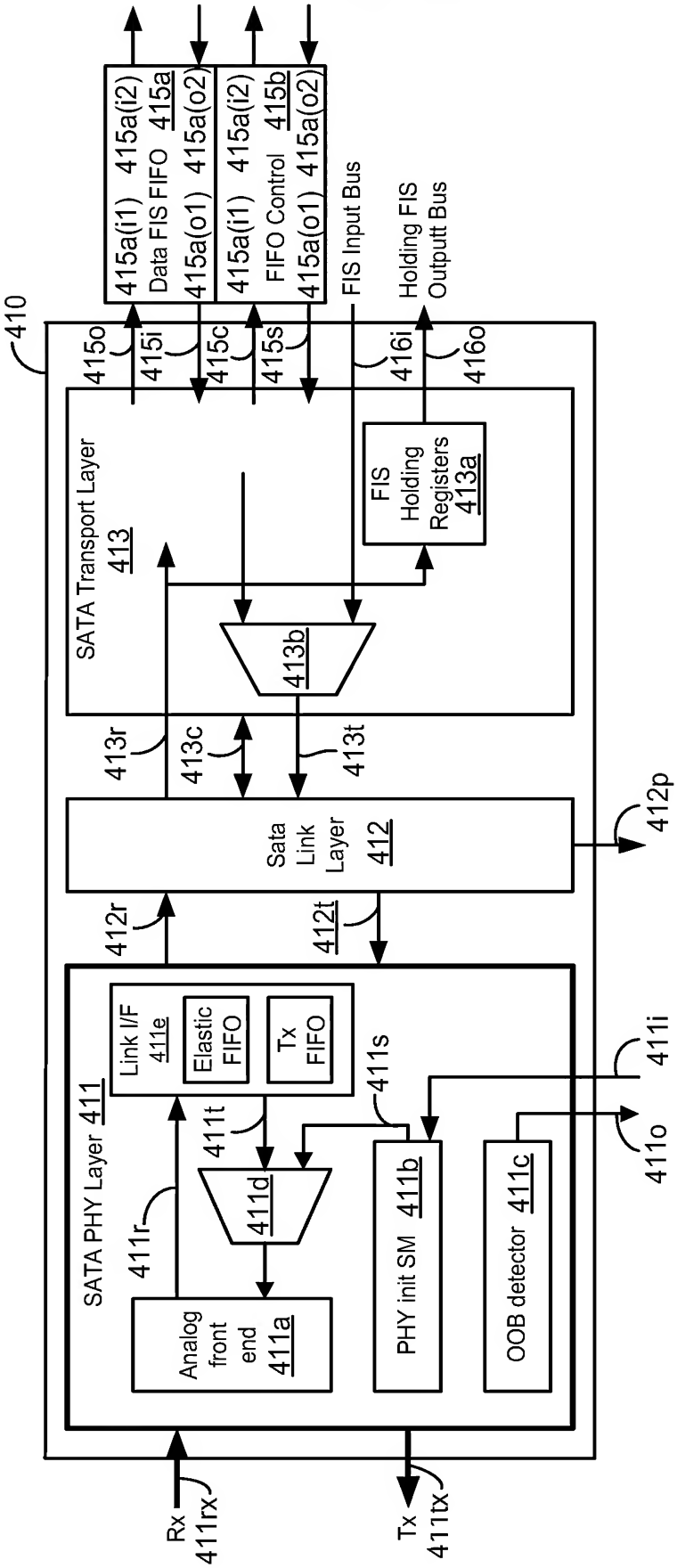

410
415a(i1) 415a(i2)
Data FIS FIFO 415a
415a(o1) 415a(o2)
415a(i1) 415a(i2)
FIFO Control 415b
415a(o1) 415a(o2)
FIS Input Bus
Holding FIS Outputt Bus
415o
415i
415c
415s
416i
416o
SATA Transport Layer 413
FIS Holding Registers 413a
413b
413r
413c
413t
Sata Link Layer 412
412p
412r
412t
SATA PHY Layer 411
Link I/F 411e
Elastic FIFO
Tx FIFO
411t
411s
411i
411o
411d
411r
Analog front end 411a
PHY init SM 411b
OOB detector 411c
Rx 411rx
Tx 411tx

FIG. 9

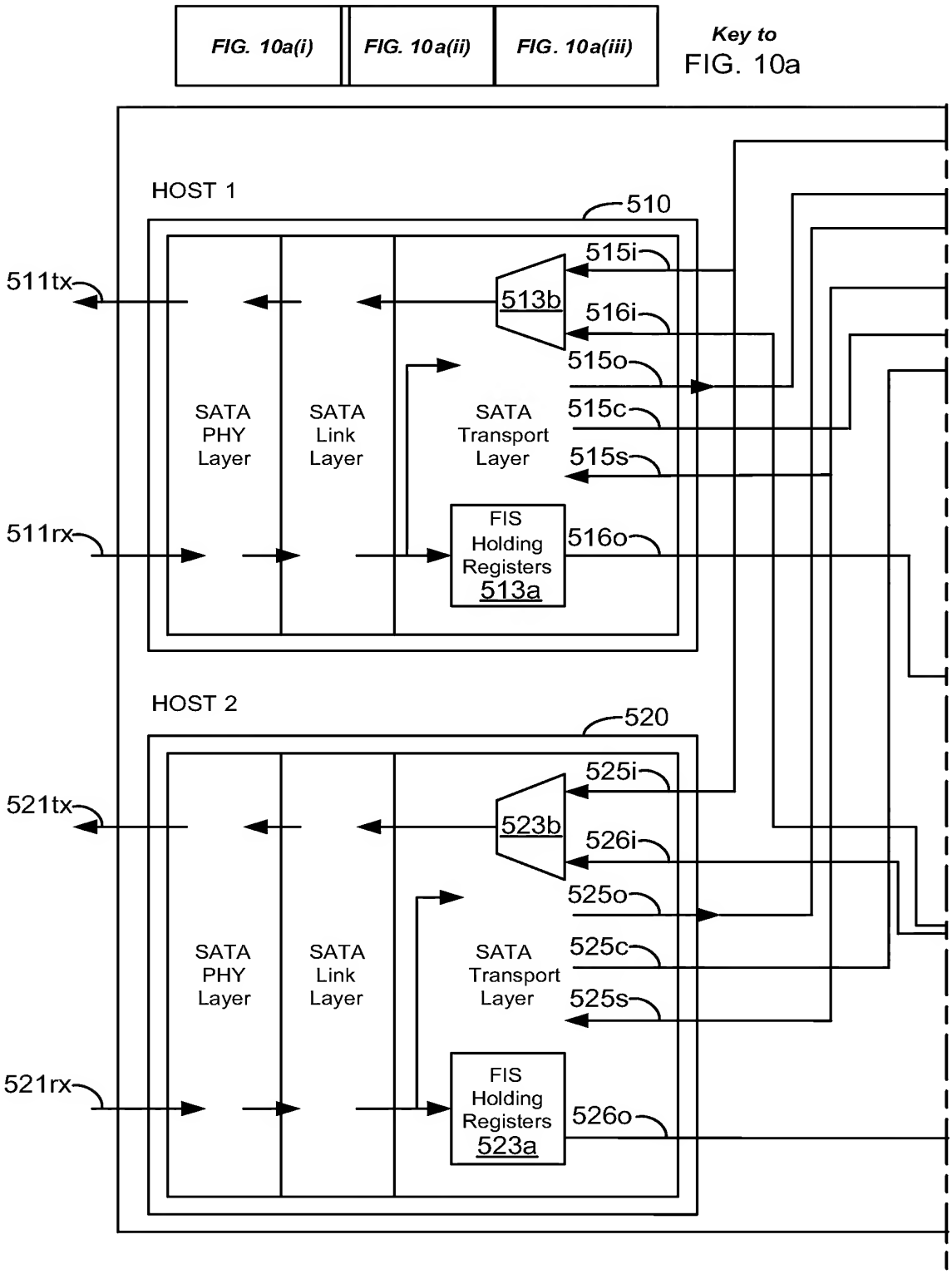


FIG. 10a(i)
FIG. 10a(ii)
FIG. 10a(iii)
Key to
FIG. 10a
HOST 1
510
511tx
511rx
513b
515i
516i
515o
515c
515s
516o
SATA
PHY
Layer
SATA
Link
Layer
SATA
Transport
Layer
FIS
Holding
Registers
513a
HOST 2
520
521tx
521rx
523b
525i
526i
525o
525c
525s
526o
FIS
Holding
Registers
523a

FIG. 10a(i)

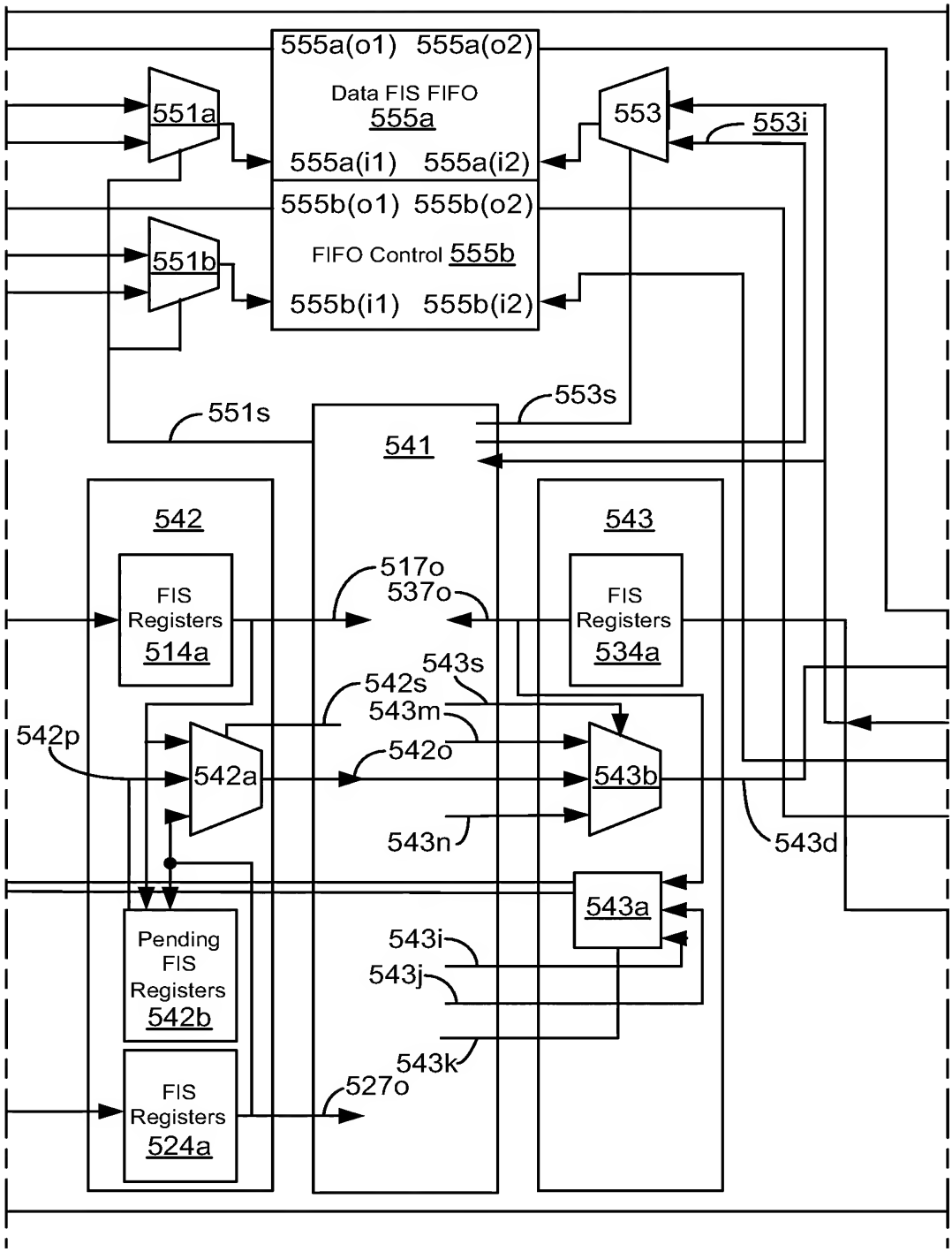

555a(o1) 555a(o2)
Data FIS FIFO
555a
555a(i1) 555a(i2)
555b(o1) 555b(o2)
FIFO Control 555b
555b(i1) 555b(i2)
551a
551b
553
553i
551s
553s
541
542
543
FIS Registers 514a
FIS Registers 534a
517o
537o
543s
542s
543m
542o
542p
542a
543b
543n
543d
543a
543i
543j
543k
Pending FIS Registers 542b
FIS Registers 524a
527o

FIG. 10a(ii)

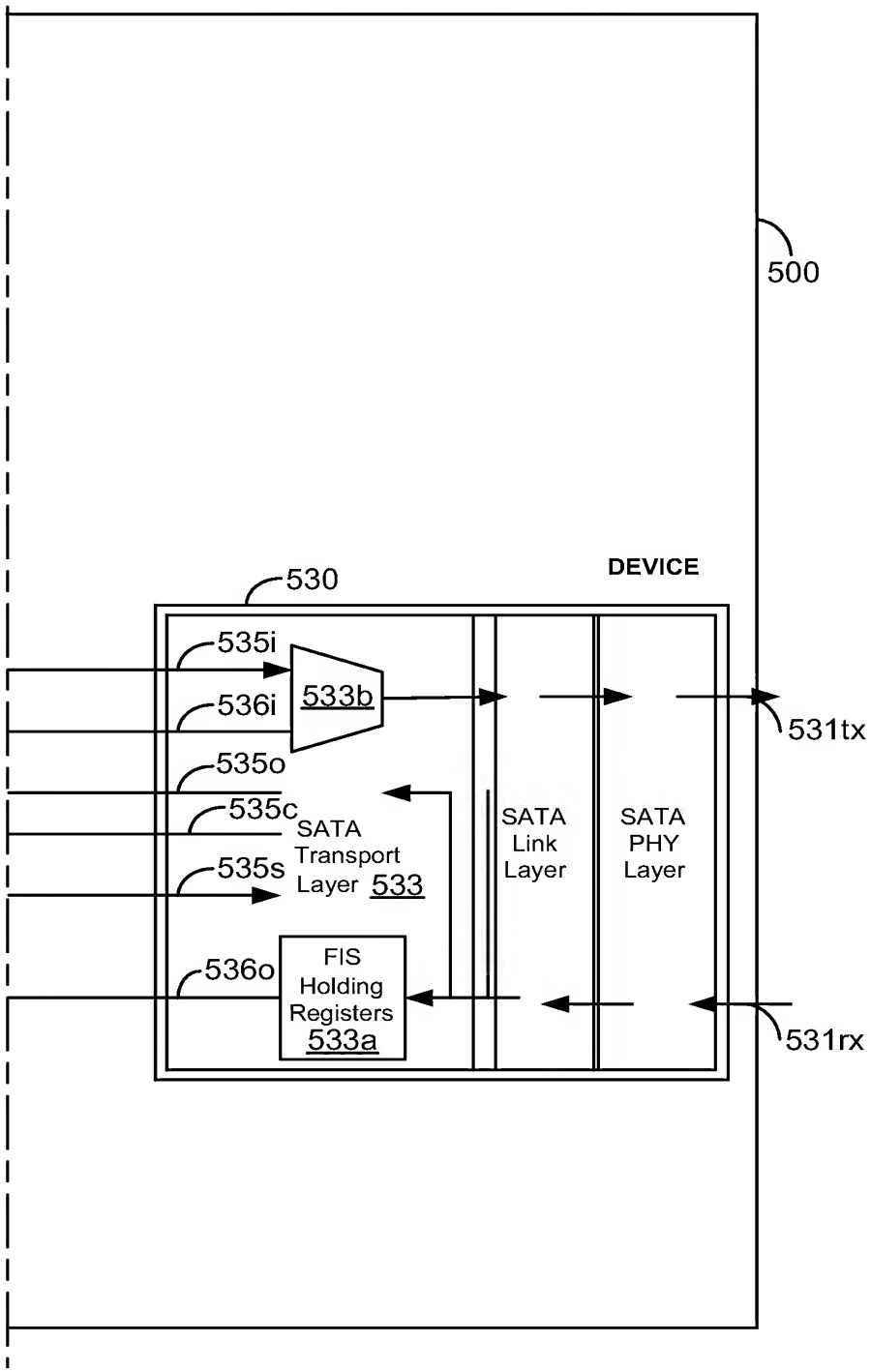

500
DEVICE
530
535i
536i
533b
535o
535c
SATA
Transport
Layer 533
535s
536o
FIS
Holding
Registers
533a
SATA
Link
Layer
SATA
PHY
Layer
531tx
531rx

FIG. 10a(iii)

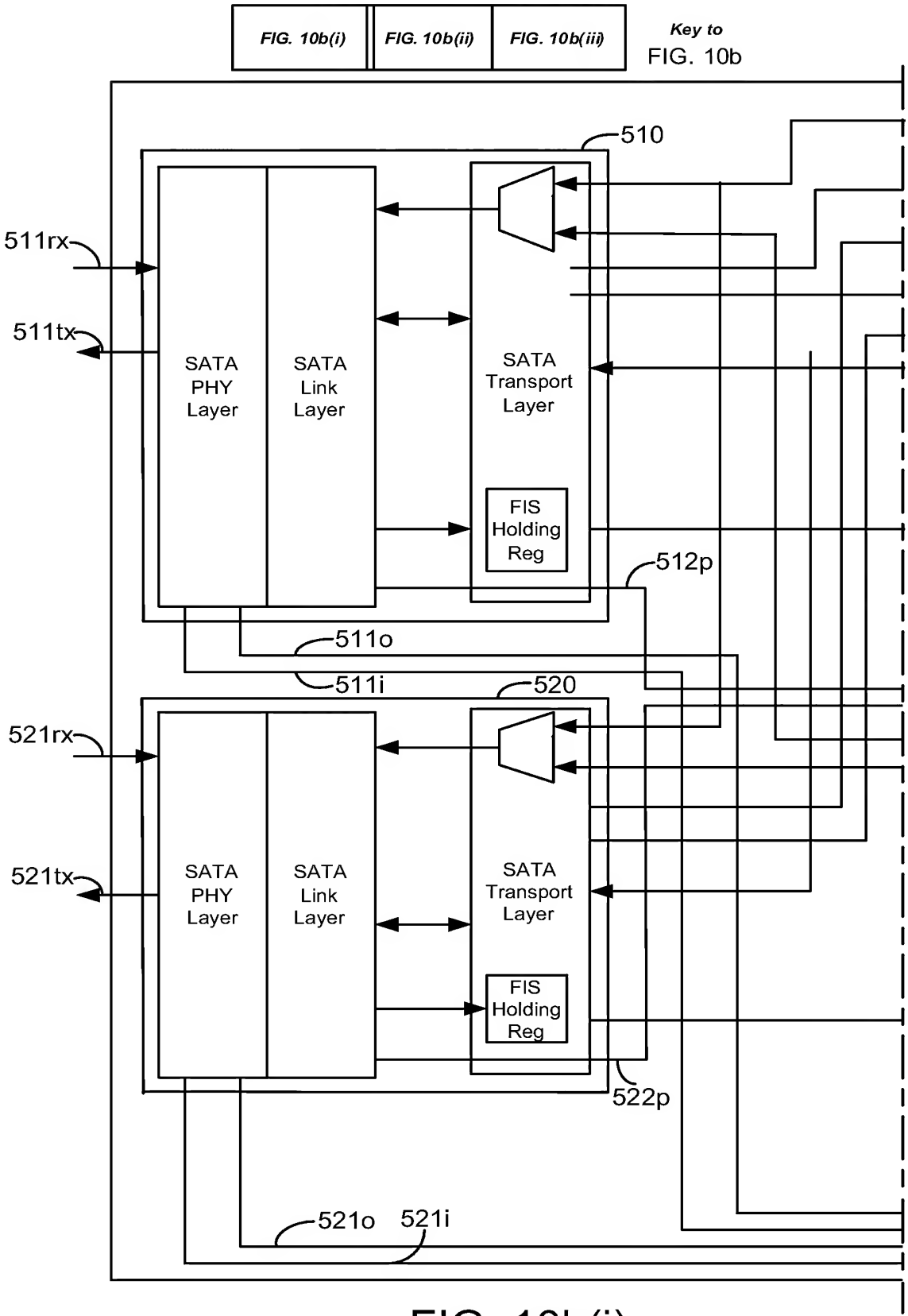


FIG. 10b(i)
FIG. 10b(ii)
FIG. 10b(iii)
Key to
FIG. 10b
510
511rx
511tx
SATA
PHY
Layer
SATA
Link
Layer
SATA
Transport
Layer
FIS
Holding
Reg
512p
511o
511i
520
521rx
521tx
SATA
PHY
Layer
SATA
Link
Layer
SATA
Transport
Layer
FIS
Holding
Reg
522p
521o
521i

FIG. 10b(i)

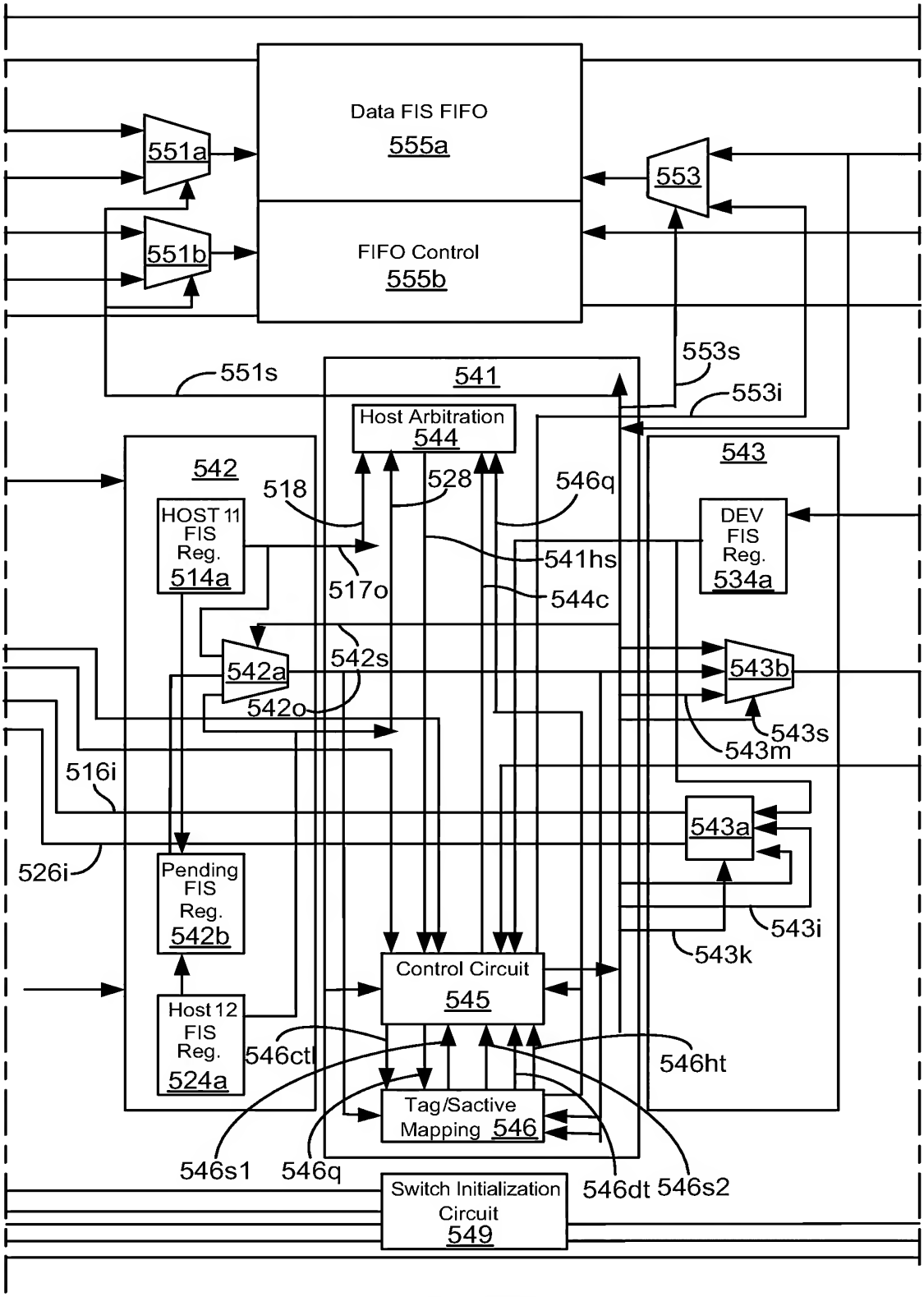

Data FIS FIFO
555a
FIFO Control
555b
551a
551b
553
551s
541
553s
553i
Host Arbitration
544
542
543
518
528
546q
HOST 11 FIS Reg.
514a
DEV FIS Reg.
534a
541hs
517o
544c
542a
542s
543b
542o
543s
543m
516i
543a
526i
Pending FIS Reg.
542b
543i
543k
Control Circuit
545
Host 12 FIS Reg.
524a
546ctl
546ht
Tag/Sactive Mapping 546
546s1
546q
546dt
546s2
Switch Initialization Circuit
549

FIG. 10b(ii)

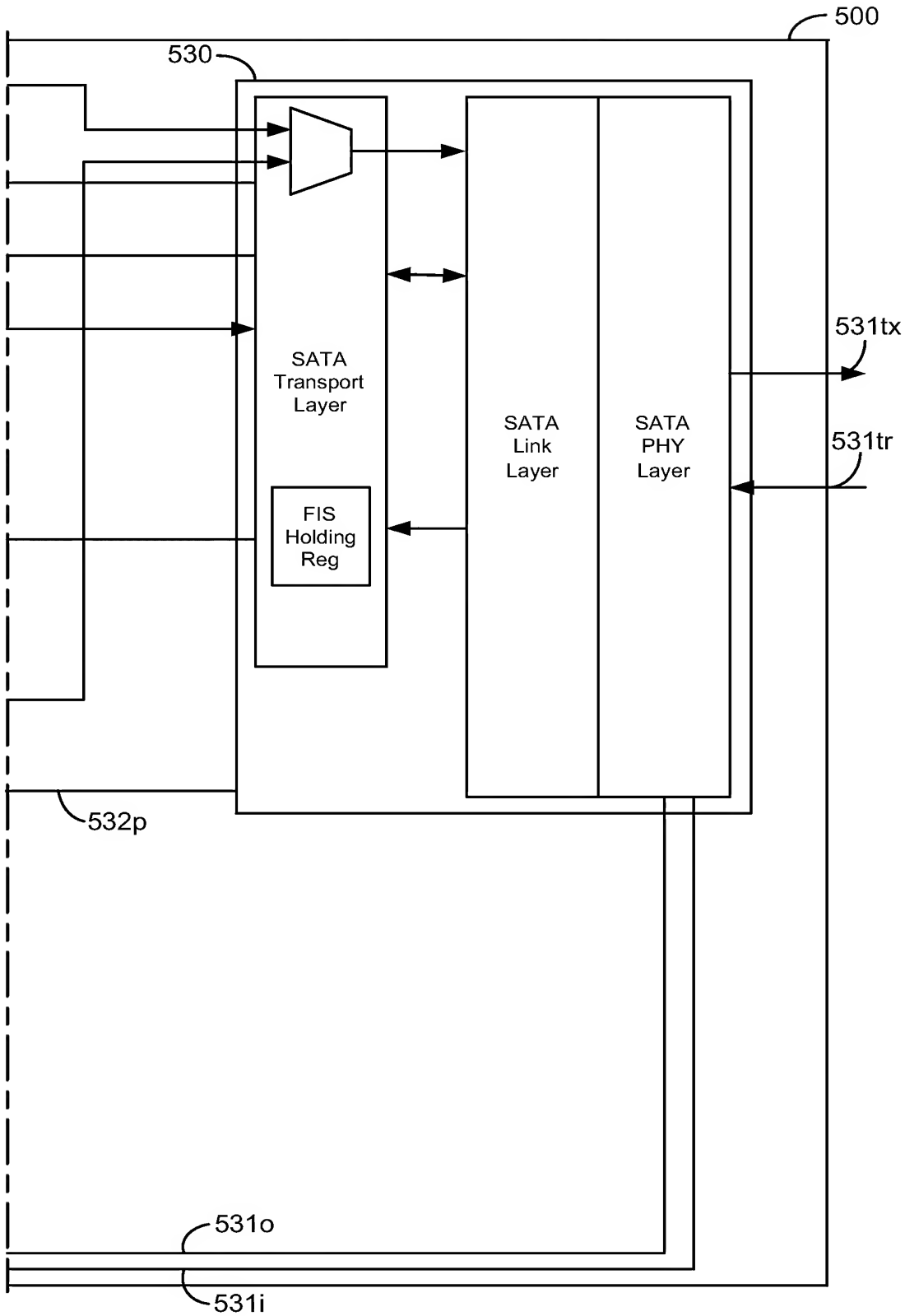
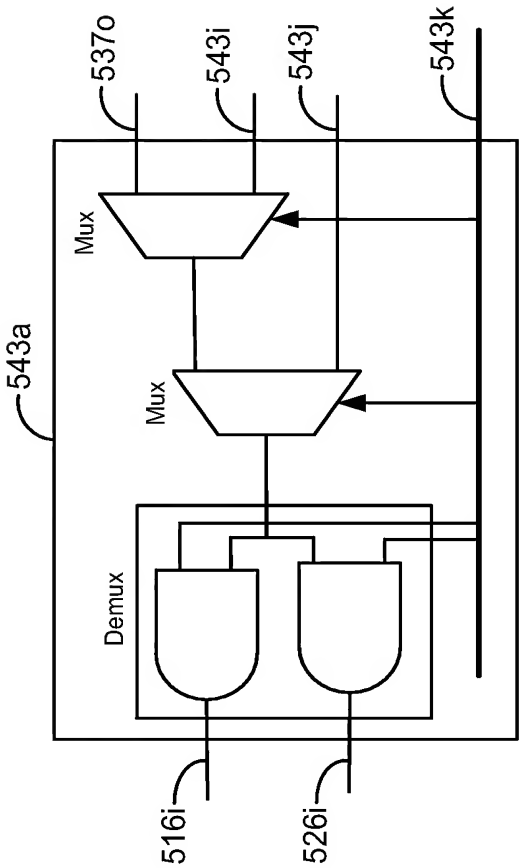

500
530
SATA
Transport
Layer
FIS
Holding
Reg
SATA
Link
Layer
SATA
PHY
Layer
531tx
531tr
532p
531o
531i

FIG.10b(iii)


537o
543i
543j
543k
Mux
Mux
543a
Demux
516i
526i

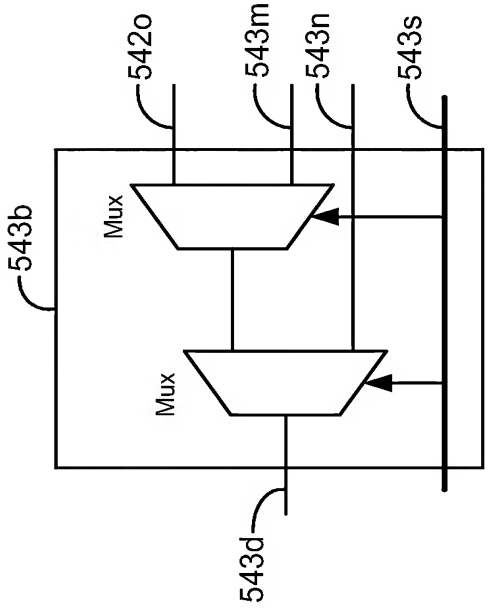

542o
543m
543n
543s
543b
Mux
Mux
543d

FIG.10c

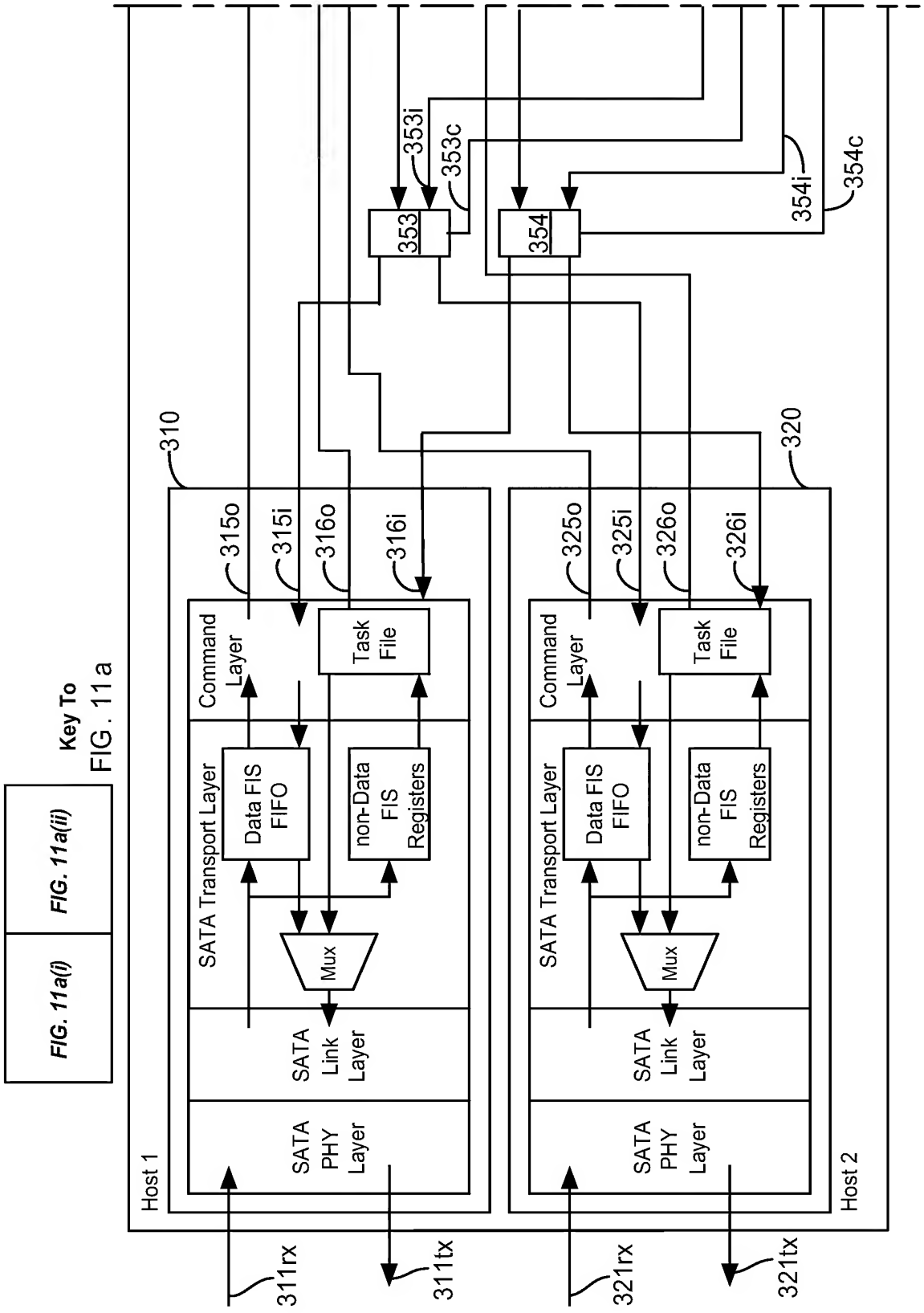

Key To
FIG. 11a
FIG. 11a(i)
FIG. 11a(ii)
Host 1
Host 2
310
320
315o
315i
316o
316i
325o
325i
326o
326i
353
354
353i
353c
354i
354c
Command Layer
Task File
SATA Transport Layer
Data FIS FIFO
non-Data FIS Registers
Mux
SATA Link Layer
SATA PHY Layer
311rx
311tx
321rx
321tx

FIG.11a(i)

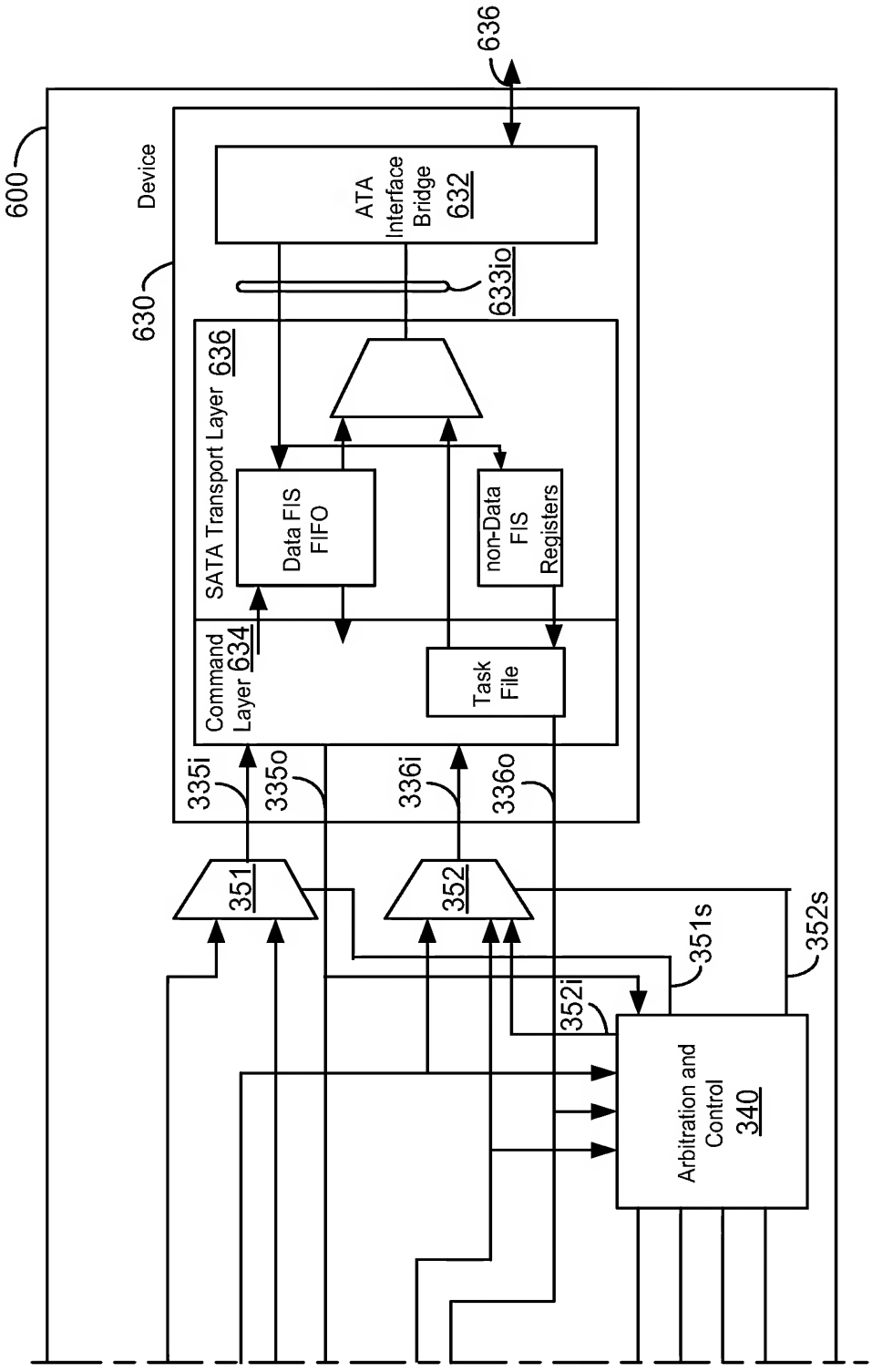

600
Device
630
636
ATA Interface Bridge 632
633io
SATA Transport Layer 636
Data FIS FIFO
non-Data FIS Registers
Command Layer 634
Task File
335i
335o
336i
336o
351
352
351s
352s
352i
Arbitration and Control 340

FIG.11a(ii)

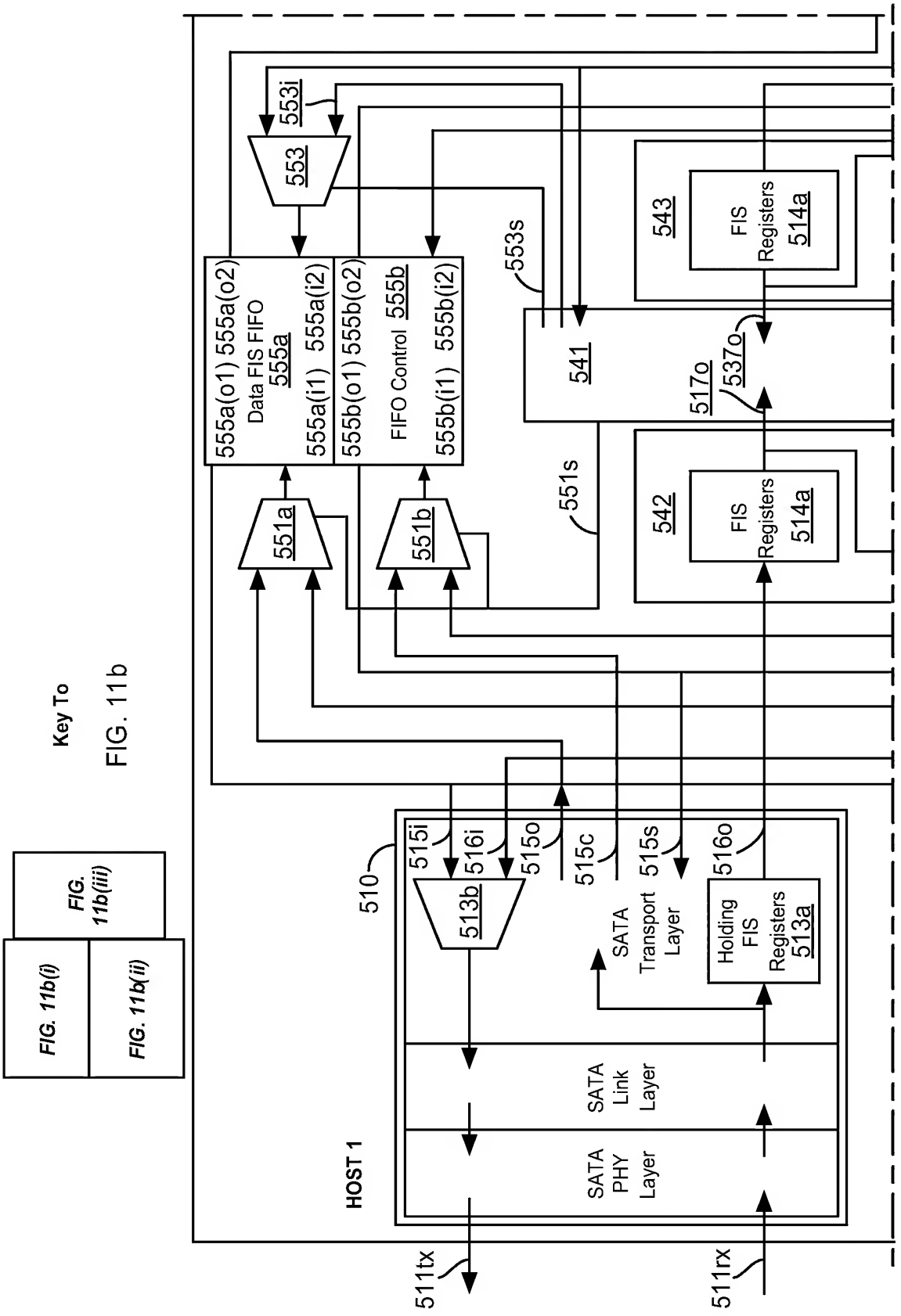


FIG.11b(i)

Key To

FIG. 11b

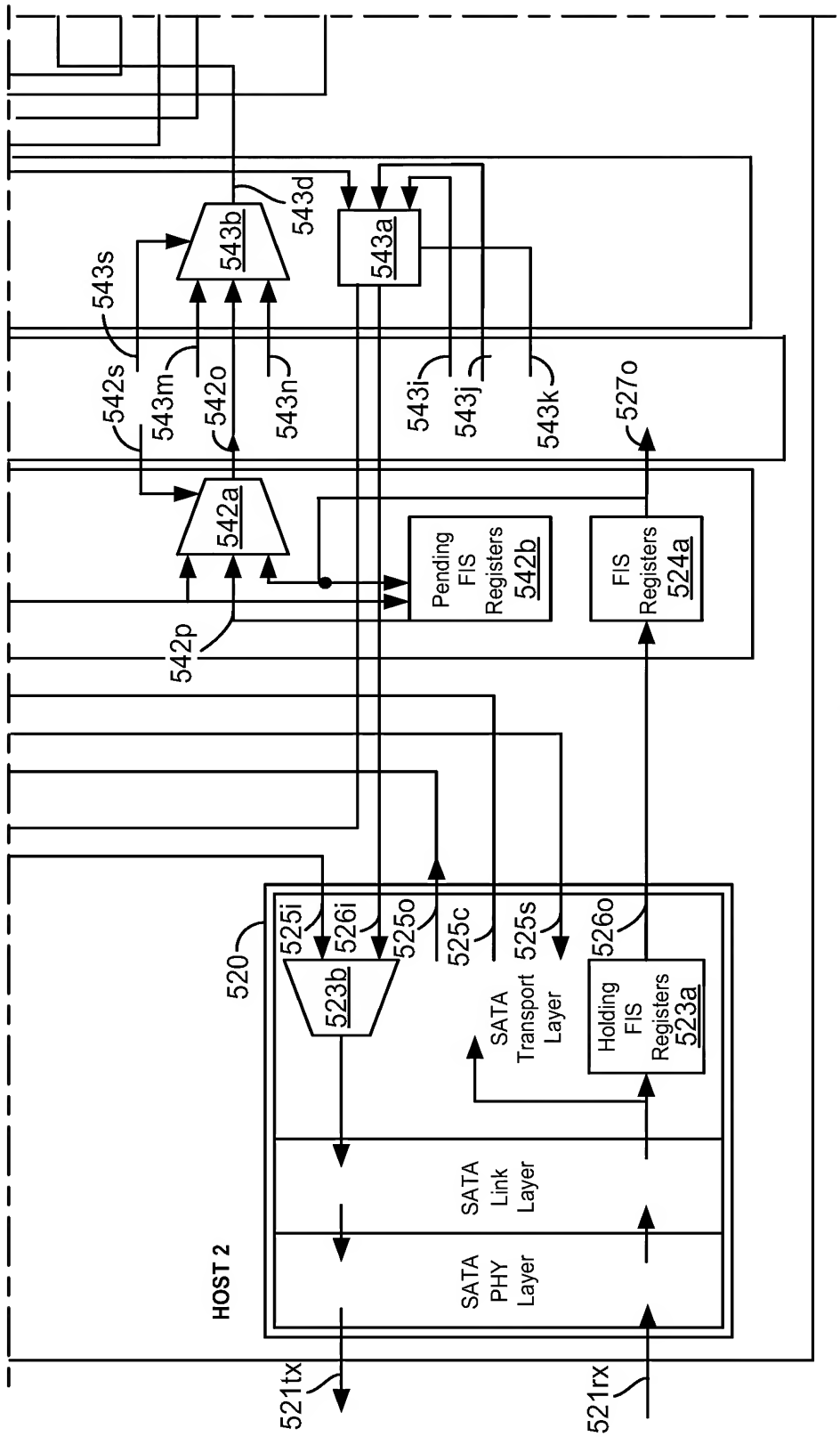

543d
543b
543a
543s
542s
543m
542o
543n
543i
543j
543k
527o
542a
542p
Pending FIS Registers 542b
FIS Registers 524a
520
525i
526i
525o
525c
525s
526o
523b
SATA Transport Layer
Holding FIS Registers 523a
SATA Link Layer
SATA PHY Layer
HOST 2
521tx
521rx

FIG.11b(ii)

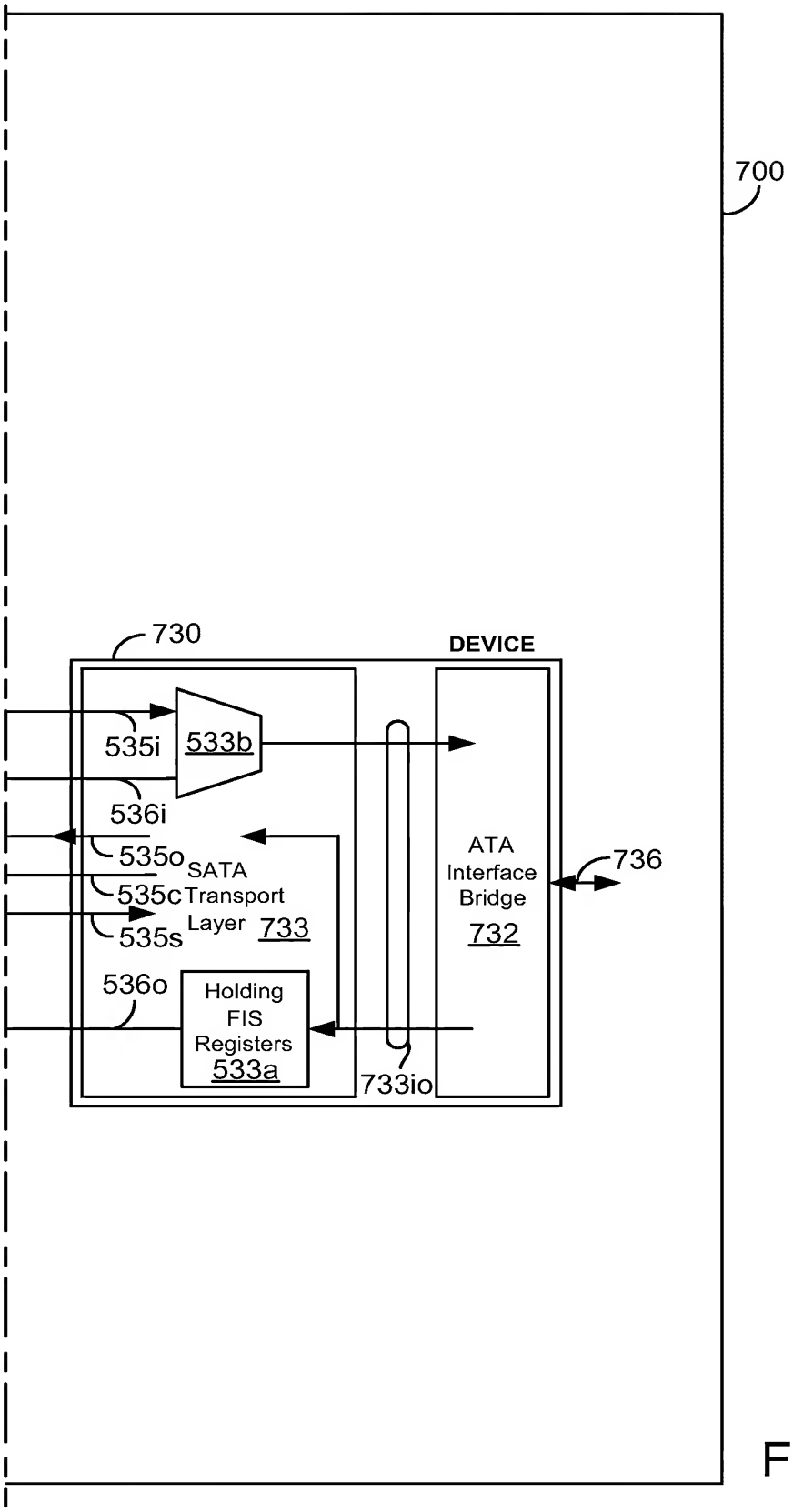

700
730
DEVICE
535i
533b
536i
535o
SATA
Transport
Layer
733
535c
535s
536o
Holding
FIS
Registers
533a
733io
ATA
Interface
Bridge
732
736

FIG.11b(iii)

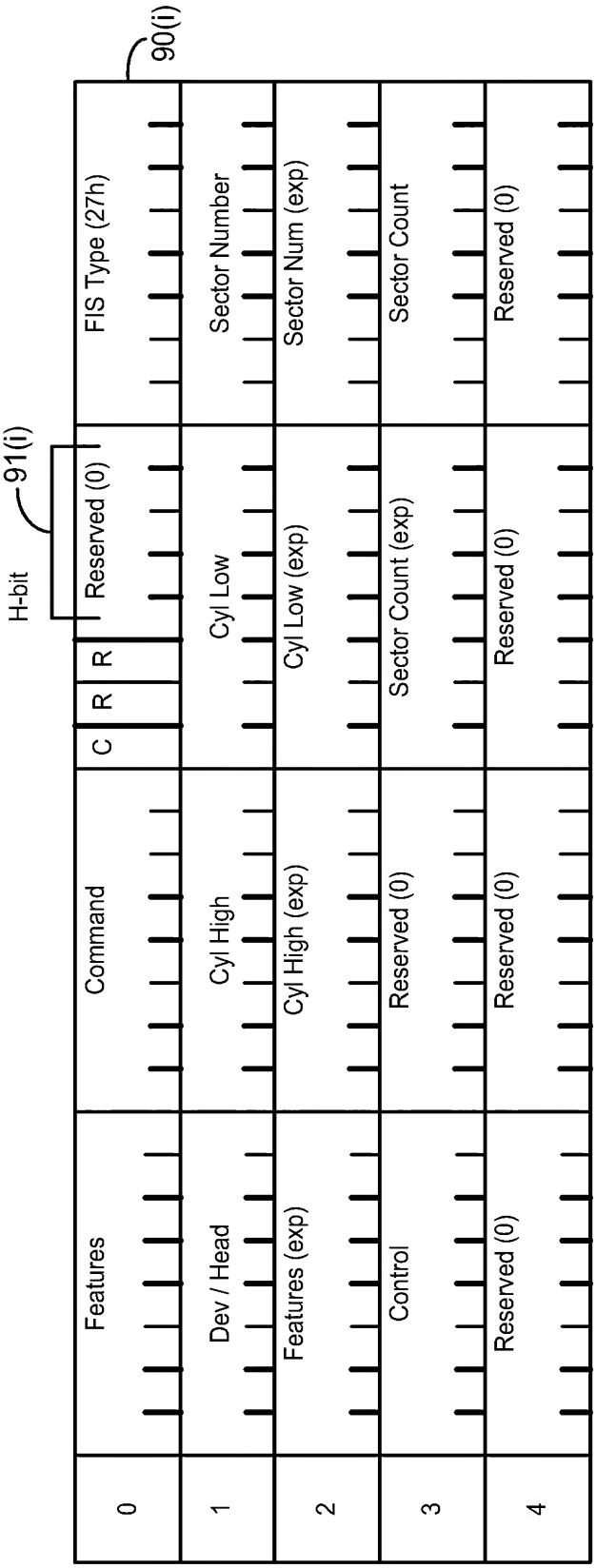


FIG. 12(i) Register FIS Host to Device

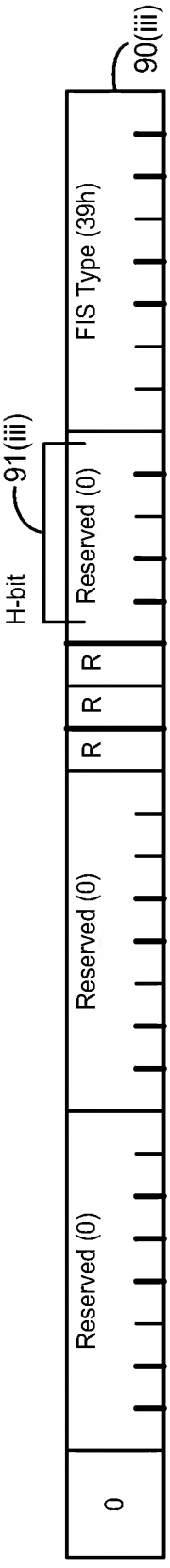


FIG. 12(iii) DMA Activate FIS, Device to Host

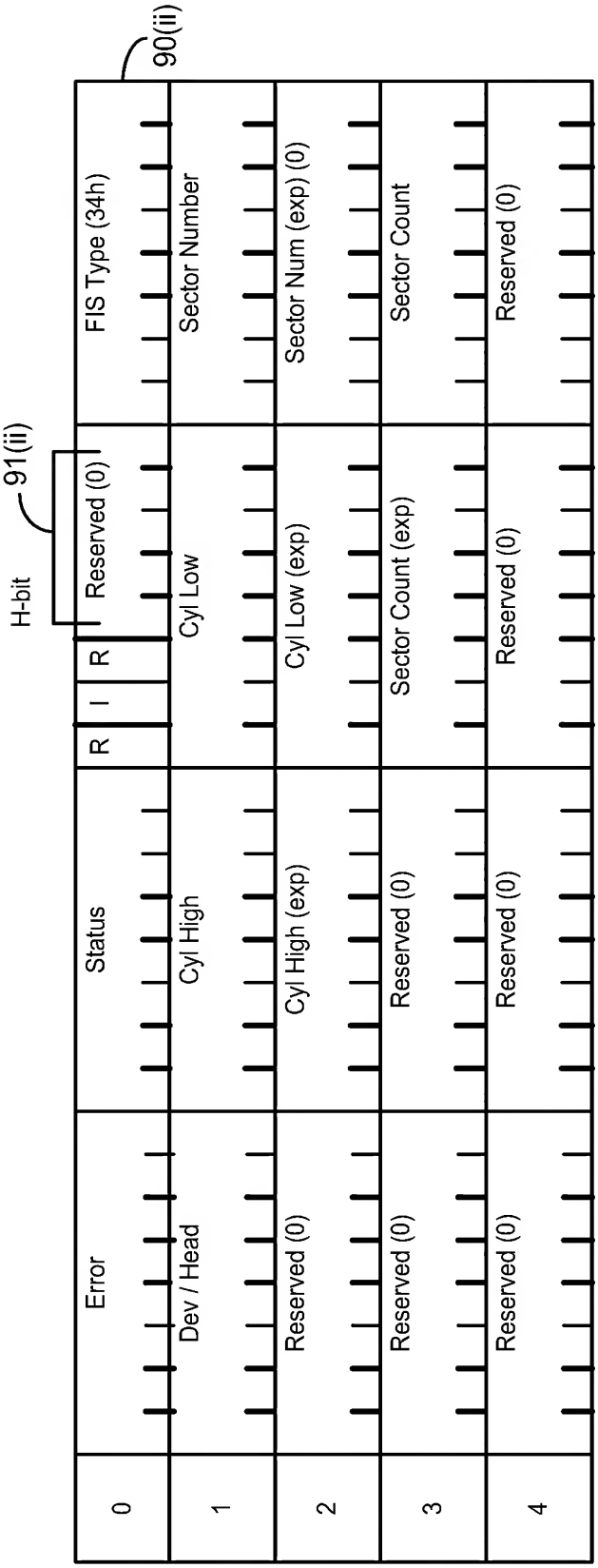


FIG. 12(ii) Register FIS Device to Host

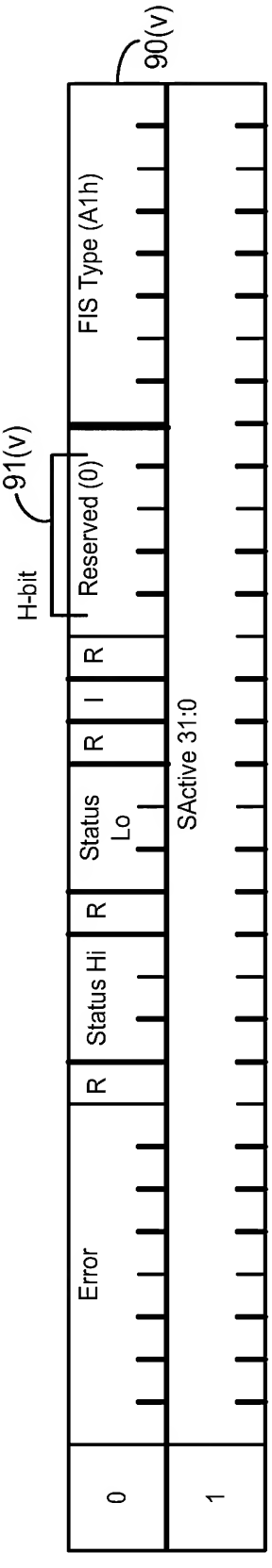


FIG. 12(v) Set Device Bits FIS

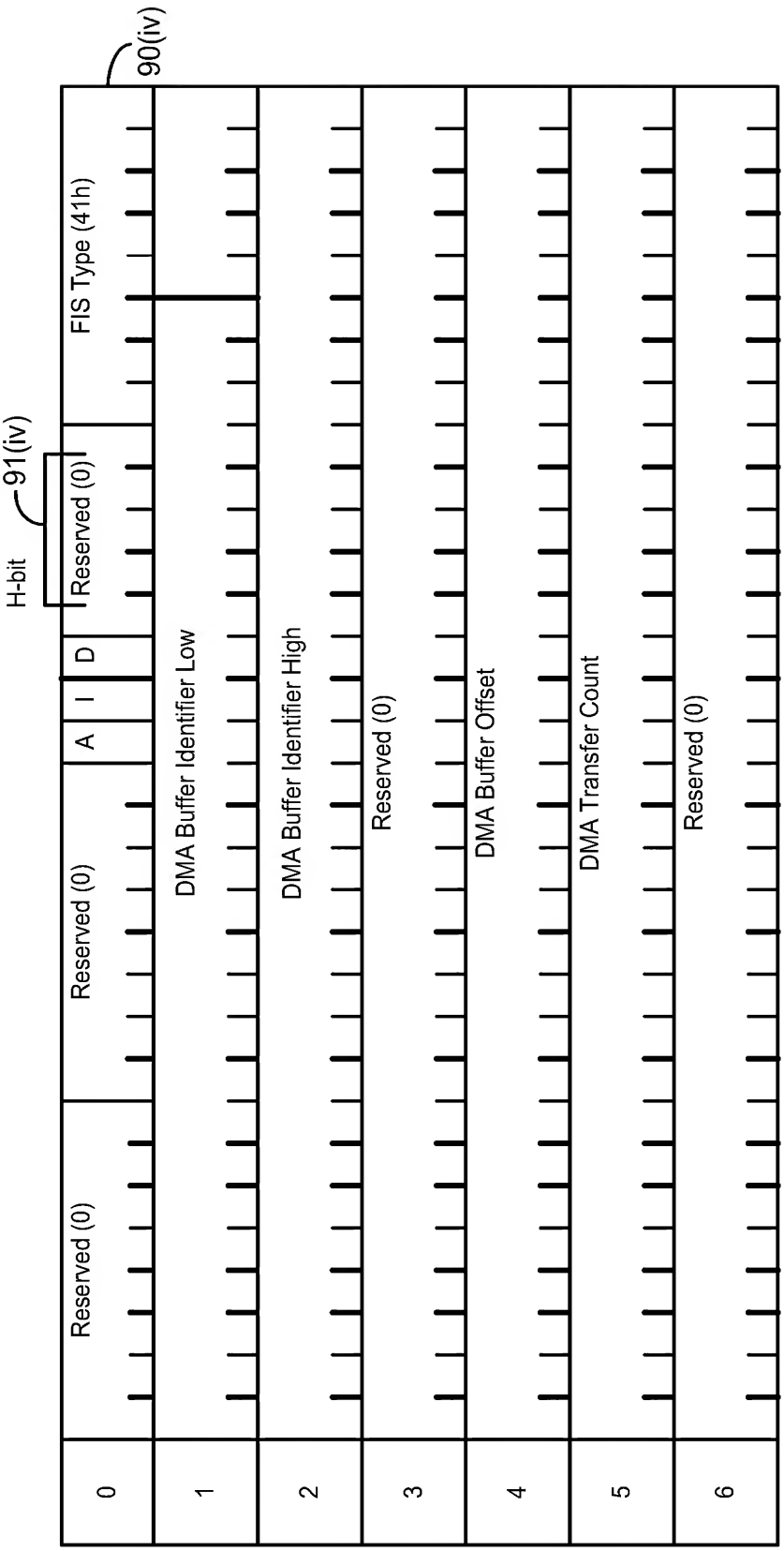


FIG. 12(iv) DMA Setup FIS

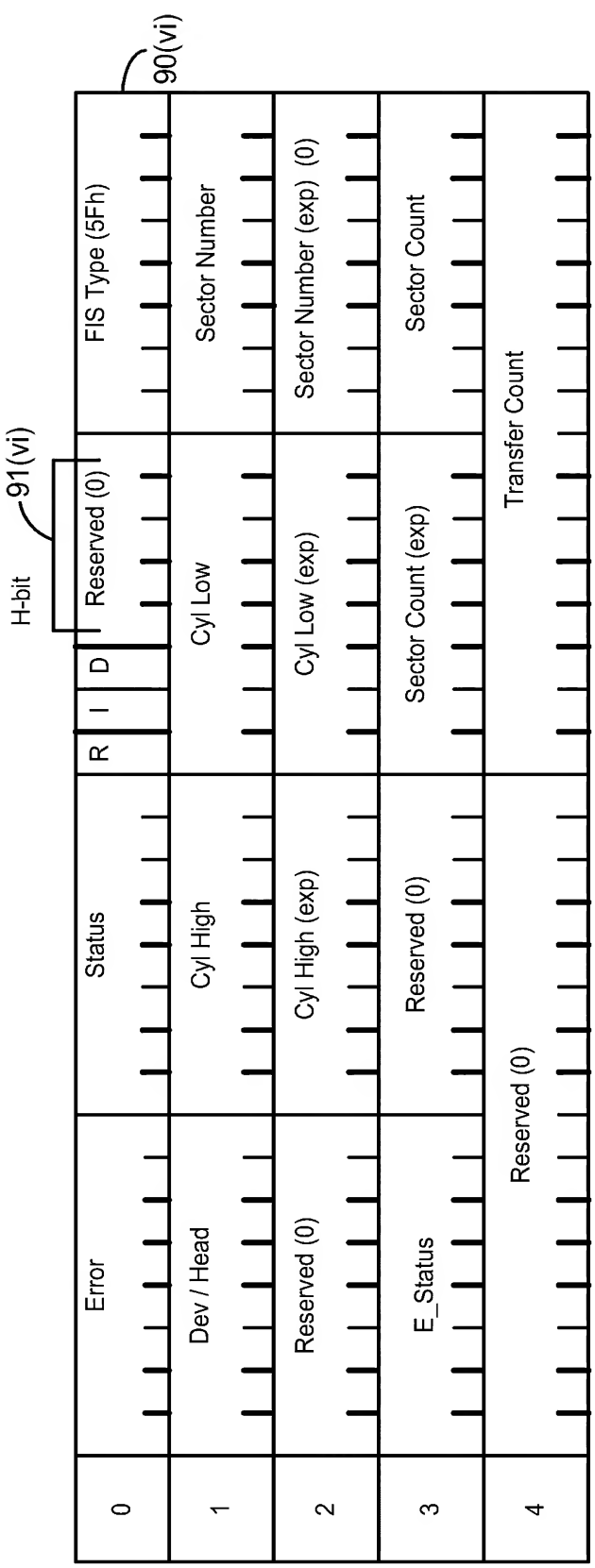


FIG. 12(vi) PIO Setup FIS

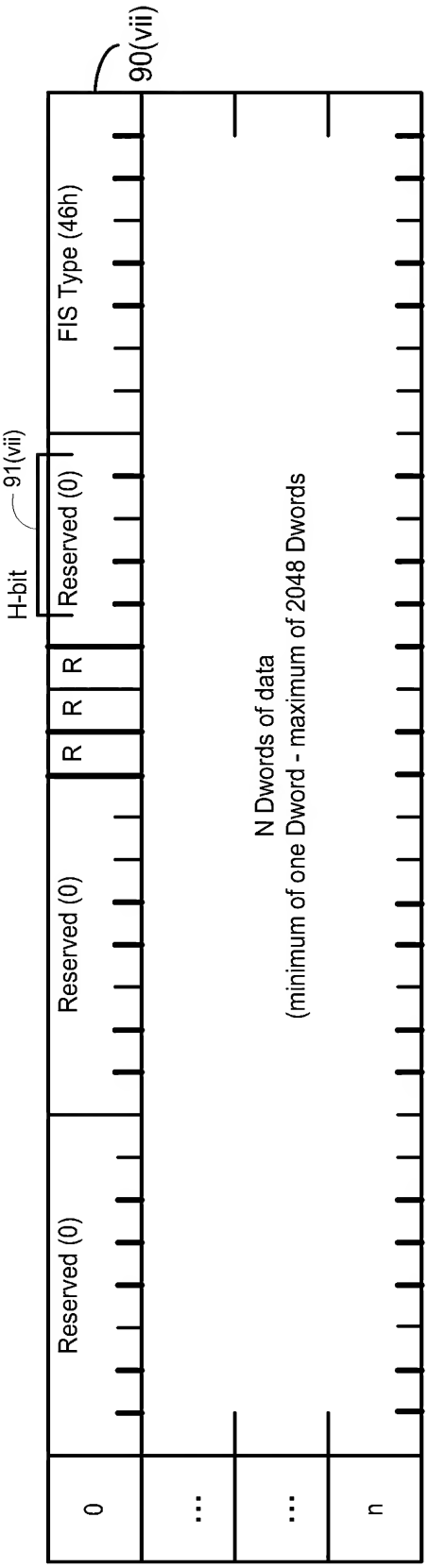


FIG. 12(vii) Data FIS

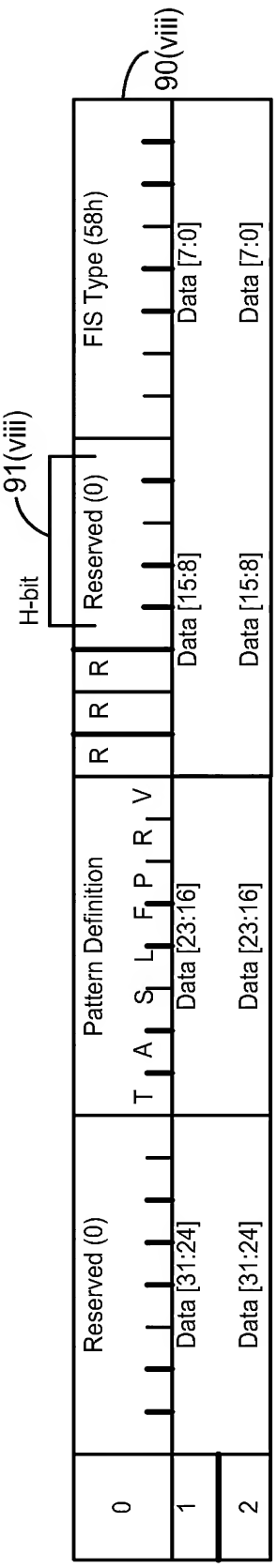


FIG. 12(viii)BIST Activate FIS